SMT J-Lead VI Chip® Soldering Recommendations

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SMT J-lead, Half and Full VI Chip packages

Introduction

VI Chip products are intended for reflow soldering assembly. The information contained in this document defines the processing conditions required for successful attachment to a PCB. Failure to follow the recommendations provided can result in aesthetic defects, as well as device failure or reduced reliability due to compromised solder joint integrity.

VI Chip Package Description

The VI Chip is an overmolded power component with electrical connections and mechanical attachment to the PCB provided using J-leads on two sides of the package. The J-lead typically forms an oblique angle with the bottom portion soldered to the PCB and the top portion attached to the VI Chip. For more information about the J-lead see the Post-Reflow Inspection section in this application note.

- Refer the package drawing provided in the product data sheet.
- Recommended footprint is specified in the package outline drawing.
- Plated surface finish is specified in the product data sheet.
- MSL rating and number of permitted reflows are specified in the product data sheet.

MSL Handling

VI Chip device Moisture Sensitivity Level (MSL) is a function of the peak reflow temperature to which the components will be exposed during the reflow operation. Components should remain in the dry vacuum bag during storage prior to assembly. Exposure to ambient humidity for periods longer than those specified in Table 1 will require that the component is baked at 125°C for 48 hours prior to assembly to remove moisture from the package. VI Chip modules may be baked multiple times to remove moisture; however the maximum bake temperature should not exceed 125°C.

Exposure time to ambient humidity conditions between reflow cycles is considered cumulative; therefore if a VI Chip module is to be exposed to a reflow soldering process multiple times, care must be taken to ensure that the total exposure time to ambient conditions does not exceed the MSL rating for the device

Failure to follow the MSL handling listed on the data sheet or the bake procedure may result in damage to the VI Chip package incurred during the reflow procedure. This damage could include package blistering, delamination, or internal solder shorting resulting in loss of electrical functionality or reduced operating life. Internal damage may occur which is not visible by external inspection.

Table 1
MSL ratings, peak reflow temperature and maximum number of reflows for VI Chip product

Peak Case Temperature During Reflow (Per JEDEC J-STD-020)	Moisture Sensitivity Level	Cumulative Exposure Time to Ambient Conditions Before Bake Process is Required (hours)	Number of Reflows at this Condition
225°C	5	48	3
245°C	6	4	3
	4	72	3

Solder Process Design

Solder Paste Stencil Design

The VI Chip® J-leads are coplanar to within 4 mils (0.004in). For this reason the absolute minimum solder paste thickness is 6mils. An acceptable solder joint must have a bond line that is much greater than 0.002 inches in length. This may require the solder paste to be thicker than 6 mils to account for flux content and transfer efficiency. The stencil apertures should be 0.9:1.

For 225°C reflow: 63/37 SnPb, either no-clean or water-washable solder paste should be used. Other types of SnPb solder pastes may be used provided the device can be safely reflowed without exceeding its maximum case temperature.

For 245°C (lead free) reflow: SAC 305, either no-clean or water-washable solder paste should be used. Other types of lead-free solder pastes may be used if the module can be safely reflowed without exceeding its maximum case temperature.

Pick-and-Place

The VI Chip modules should be placed within ±5 mils. To maintain placement position, the modules should not be subjected to acceleration greater than $500in/s^2$ between pick-and-place and reflow. Pick-and-place z-axis pressure and dwell time after placement should be optimized to insure proper seating in the solder paste and adequate wetting during reflow. All people or equipment handling VI Chip modules should have proper ESD protection to avoid damaging the units during the mounting process.

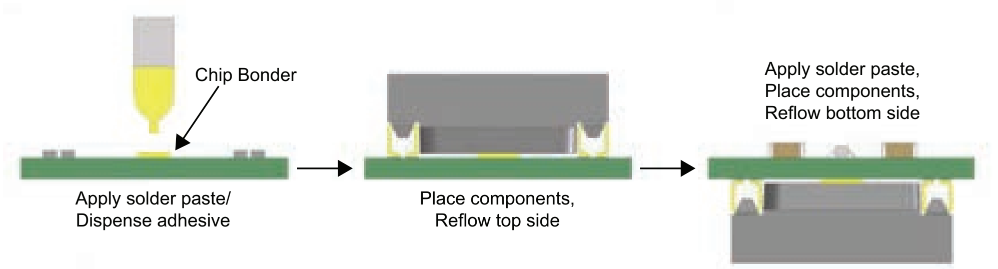
Solder Reflow Method

A forced-air convection oven is recommended for reflow attachment of VI Chip modules. Other types of reflow methods (Vapor Phase, IR, etc.) have not been qualified for use with VI Chip modules and should be studied to ensure that the unit's maximum case temperature, time above liquidus, or temperature gradient is not exceeded during reflow.

Chip Bonder Adhesive Application

Background: A chip bonder adhesive epoxy should be used to hold the VI Chip module in place if exposed to subsequent reflow conditions after the initial reflow. In addition, engineering best practices supports the use of the chip bonder adhesive to relieve mechanical stress from the J-lead solder joints. The epoxy is dispensed on the PCB after the solder screen printing process before the VI Chip module is placed on the board and subjected to solder reflow (as shown on next page).

Figure 1
Dispensing process flow



Chip Bonder Epoxy Selection Criteria

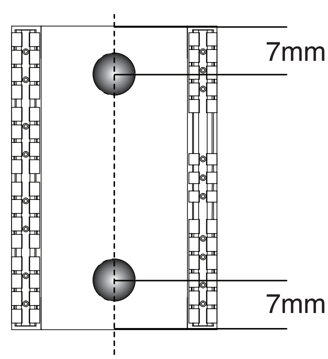
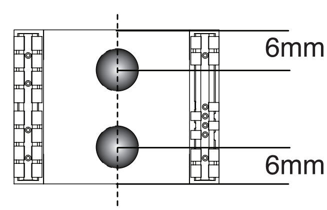
Vicor recommends the Loctite 3621 or similar surface mount adhesives for use in attaching VI Chip® modules to the PCBs. The epoxy adhesive is cured during the solder reflow and can be cured using either the leaded or the lead-free reflow profiles. Preferred properties of the chip bonder adhesives for this application include:

- One component adhesive (no mixing)
- Minimum bleed
- Low cure temperature
- Removable
- Non-electrically conductive
- Automatically dispensing capability

Dispensing Details

A two-dot pattern should be used under the VI Chip module as illustrated in Figure 2 below. The recommended dispense weight per dot is 5mg. For full-size VI Chip modules, each dot is deposited 7mm from the nearest edge of the VI Chip module on the center vertical axis. For half-size VI Chip modules, each dot is deposited 6mm from the nearest edge of the VI Chip module on the center vertical axis (as shown below).

Figure 2
Recommended chip bonder dispense pattern for VI Chip modules (BCM® Bus Converter / VTM™ Current Multiplier footprints shown, same dispense pattern applies)

Dispense Pattern	
Full-size VI Chip module	Half-size VI Chip module
	

225°C Reflow Procedure

If noted in the data sheet as 225°C reflow capable, the VI Chip® module is qualified per J-STD-020D.1 for three reflows at a peak temperature of 225°C. Please refer to the individual product data sheet for the MSL level for a particular reflow temperature. Recommendations provided here are based on experiments executed on VI Chip modules. They do not represent exact conditions present at a customer site. Hence, these recommendations should be used as guidance only and process optimizations are recommended to develop an application-specific reflow solution. There are two temperatures critical to the reflow process: the solder joint temperature and the module case temperature. The solder joint temperature should reach a temperature conducive to proper solder reflow, while the module case temperature must not exceed 225°C at any time during reflow. The difference in temperature between joint and case temperature should be kept within 10°C throughout the entire process.

During reflow, the assembly is preheated to between 100°C and 150°C and held for a minimum of one minute to evaporate solvents from solder paste. The next stage is a soak zone where the flux activation occurs and the flux reacts with the oxide and contaminants on the surfaces to be joined. The assembly is then brought to above the 183°C liquidus temperature to produce reflow of the solder. The typical time above liquidus (183°C) is preferably 60 – 90 seconds maximum. In order to achieve the appropriate temperature profile, the peak temperature and belt speed of the reflow furnace are determined based on the total mass of the assembly going through soldering.

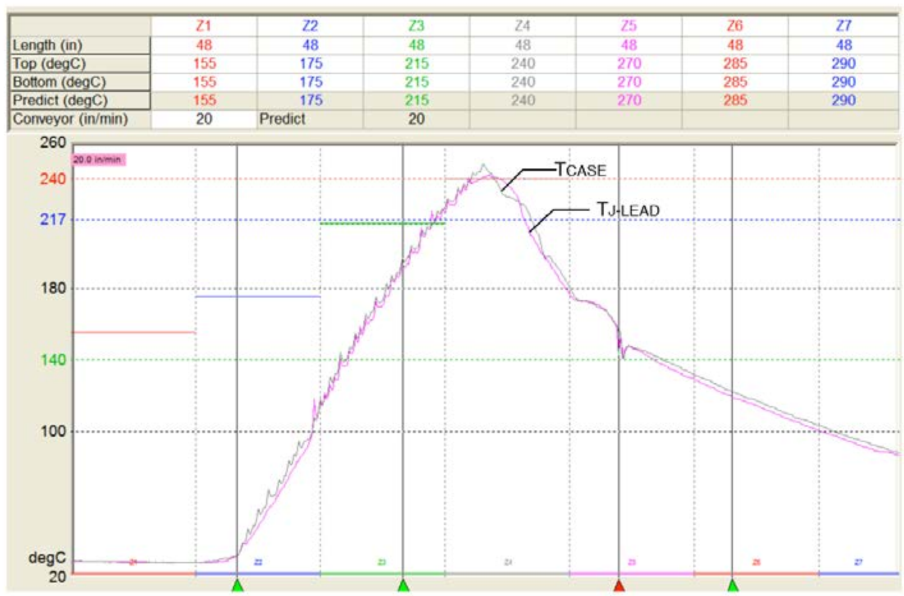
The modules can be subjected to the maximum case temperature of 225°C up to three times. MSL handling time is considered cumulative and the total time of exposure to ambient conditions, including time between reflows, should not exceed the MSL 5 limit. Exposure to ambient conditions for more than 48 hours requires a re-bake at 125°C for 48 hours prior to reflow to remove moisture. The details for the reflow profile are summarized in Table 2.

245°C Reflow Procedure

If noted in the data sheet as 245°C reflow capable, the VI Chip® modules are qualified per J-STD-020D.1 for three reflows at a peak temperature of 245°C. Again, refer to the data sheet for product specific MSL ratings. If the product is rated at MSL 6, time out of bag (TOB) should be assumed to be 4 hours unless otherwise stated. As with the 225°C reflow profile, the solder reflow recommendations provided here are based on experiments executed on VI Chip modules and do not represent exact conditions present at a customer site.

There are two temperatures critical to the reflow process: the solder joint temperature and the module case temperature. The solder joint temperature should reach a temperature conducive to proper solder reflow, while the module case temperature must not exceed 245°C at anytime during reflow.

Figure 3
Typical 245°C solder reflow profile for VI Chip module to board assembly



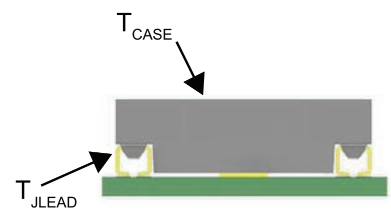
In the reflow step, the assembly should be heated at a rate no faster than 3°C/s. Once the assembly is above the liquidus temperature to produce reflow of the solder, the typical time above liquidus should be between 60 – 90 seconds maximum. In order to achieve the appropriate temperature profile, the peak temperature and belt speed of the reflow furnace are determined based on the total mass of the assembly going through soldering. The final stage is cooling. Cool down rate should be no faster than 6°C/s. Figure 3 shows a typical reflow profile used in the reflow of SAC 305 or similar solder. Between each reflow, the same MSL 6 handling procedure should be applied. Exposure to ambient conditions for more than four hours requires a re-bake at 125°C for 48 hours prior to reflow to remove moisture.

General Guidelines for Soldering

Maximum Temperature Difference across VI Chip® Package

The temperature differential across the J-lead package should be maintained at 10°C throughout the reflow process and especially during cooling shown in Figure 3. This temperature differential should be measured using at least two locations on the top and lead of the VI Chip module as shown in Figure 4 below. Maintaining a low temperature gradient across the package during reflow minimizes mechanical stresses within the package and especially along the interconnect between the J-leads and the VI Chip module. Larger gradients in temperature (>10°C) during cooling increase the likelihood of compromised solder joints leading to intermittent connections over time. With very large temperature gradients (>20°C) there is a near certainty of solder joint compromise.

Figure 4
Thermocouple location for maintaining <10°C differential across VI Chip package. The temperature profile for T_{CASE} is shown in gray in Figure 3, while the temperature profile for $T_{J\text{-}LEAD}$ is shown in the pink trace.



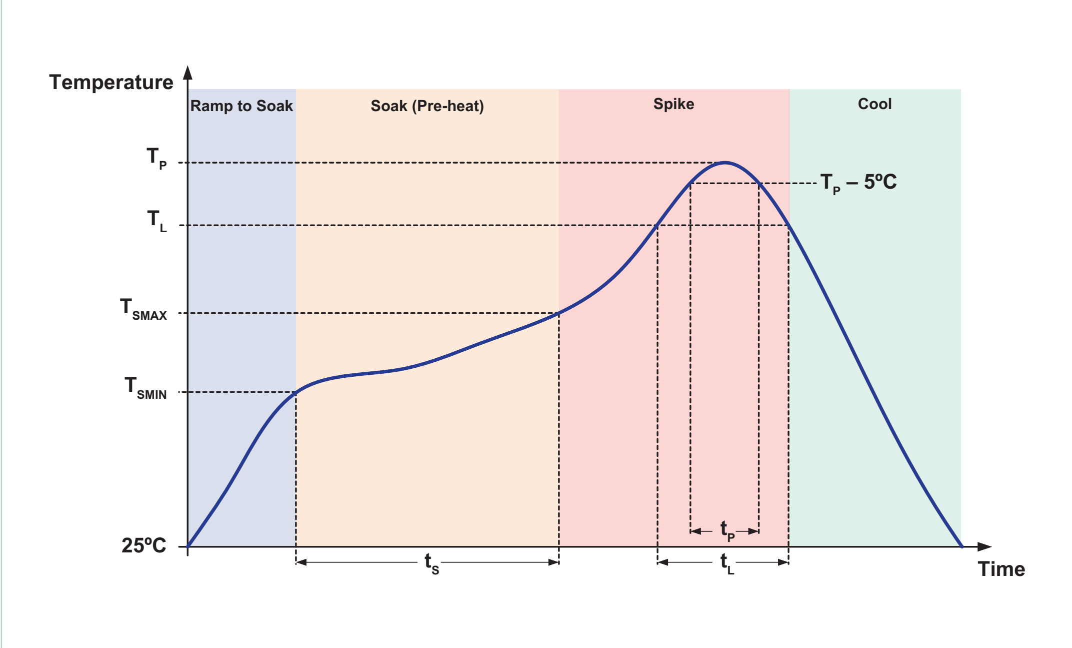
Generalized Guidelines for Convection Reflow of VI Chip Modules

Table 2 summarizes the VI Chip module recommendations for reflow parameters. Some of these parameters may be specified in individual VI Chip product data sheets. In the event of a difference between the value specified in Table 2 and the data sheet, the value in the VI Chip product data sheet supersedes the recommendation below.

Table 2
VI Chip module reflow parameter recommendations

Temperature	VI Chip Module Recommendations	
Ramp-up rate	1 – 2°C/s	
Temperature gradient (J-lead and case of VI Chip module)	10°C	
	225°C Reflow	**245°C Reflow**
Preheat temperature minimum ($T_{s\text{-}MIN}$)	120°C	170°C
Preheat temperature maximum ($T_{s\text{-}MAX}$)	150°C	210°C
Preheat time (t_s), seconds	90 – 120	90 – 120
Liquidus temperature (T_L)	183°C	217°C
Time above liquidus (t_L), seconds	60 – 90	60 – 90
Peak/classification temperature (T_P)	215°C	240°C
Time within 5°C of T_P, seconds	5 – 10	
Ramp-down rate	1 – 2°C/second	
Time 25°C to T_P	4 to 6 minutes	

Figure 5
Standard graph of critical reflow parameters (Reference: IPC/JEDEC J-STD-020C)



Post-Reflow Process

Cleaning

Following reflow, flux residue must be removed from between the VI Chip® module J-leads otherwise this residue could become electrically conductive and cause VI Chip module failures over time. Even "No-clean" flux residue can be harmful in terms of electro-migration and THB performance failures. In applications where the flux will not be cleaned following reflow, reliability tests should be performed to ensure that the long term reliability of the system is not compromised. VI Chip modules are compatible with standard water-wash procedures and most standard water-wash solvents. If there is any particular concern over a solvent compatibility with the VI Chip package, please contact Vicor Applications Engineering and provide the solvent type, intended concentration, temperature in the water-wash bath, and the relevant material data sheet(s). Depending on the solvent, a compatibility check may need to be performed.

If the VI Chip modules need to be subjected to a reflow cycle after water washing, they should first be run through a bake cycle (at least 48 hours at 125°C) to remove moisture from the package.

Inspection

Package Level: Both a package and a solder-joint inspection should be performed following a reflow operation. A package inspection should show no evidence of:

1. Solder extrusion from the VI Chip package
2. J-lead separation from the module body
3. J-lead damage or delamination
4. Top surface anomalies exceeding flatness of the VI Chip case by >0.025in or covering more than 10% of the total surface area.

Any evidence of #1, #2, or #3 would indicate that the maximum temperature was exceeded during the reflow process. Any evidence of #4 would indicate that the MSL handling guidelines were not appropriately followed.

J-lead Inspection: The VI Chip® module J-lead is a unique PCB termination, and as such, normal IPC standards cannot be applied to inspecting the quality of the solder joint. This is due to three factors summarized below:

1. The coplanarity of the array of J-leads is within 0.004in. Due to this variation, an individual J-lead that is shorter than its neighbors may not be resting on the surface of the PCB if it is supported by the taller J-leads.

2. The angle of the J-lead is specified on the VI Chip mechanical package drawing as nominally 20° with respect to the PCB surface. This angle is not controlled, however, and the actual angle will be different based on variability in the manufacturing of the J-leads. Although the range of J-lead angles is not specified, it will almost never exhibit a 0° angle with respect to the PCB (i.e., the lead is bent 90° and rests flat on the PCB) and will likewise almost never exhibit >45° angle with respect to the PCB.

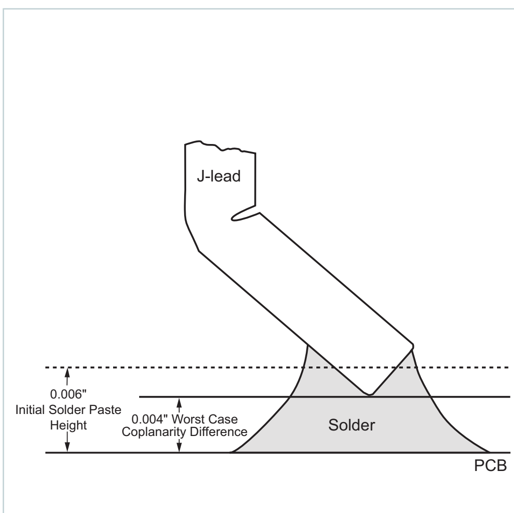
3. The VI Chip package has an inner row of J-leads that cannot be directly inspected by sight or with standard equipment.

The criteria for assessing the validity of a J-lead solder connection is that the solder bondline must greatly exceed 0.002in along the length of the lead. As a result of the coplanarity variation of the J-leads, the 0.006in of printed solder paste is crucial to ensure that a J-lead that is shallow by as much as 0.004in still has sufficient contact with the solder to form a correct bond. During the reflow process, the solder will wick up the J-lead and the resulting bond will extend further up the J-lead than the initial solder past height. As a result of the J-lead angle variation, the appearance of a good solder joint will vary greatly depending on the angle. Figures 6 thru 11 depict valid and invalid solder joints for extremes in J-lead coplanarity variation.

In each case, the difference between a valid and invalid solder joint is the presence of a bond between solder and lead of an acceptable length.

Figure 6 *(left): Example of a valid solder joint for J-lead with shallow bend (>20° angle) and worst-case (0.004in) coplanarity*

Figure 7 *(right): Example of an invalid solder joint for J-lead with shallow bend (>20° angle) and worst-case (0.004in) coplanarity*



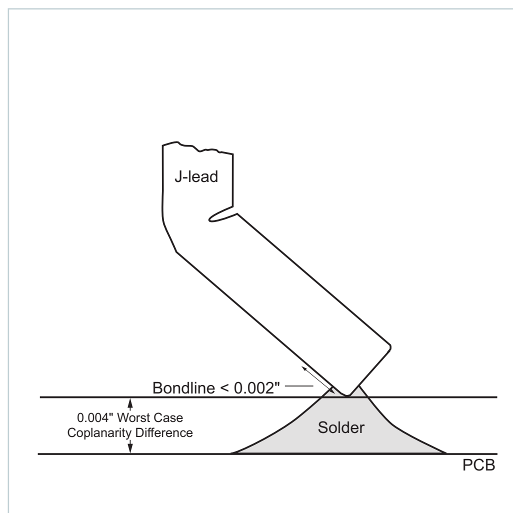
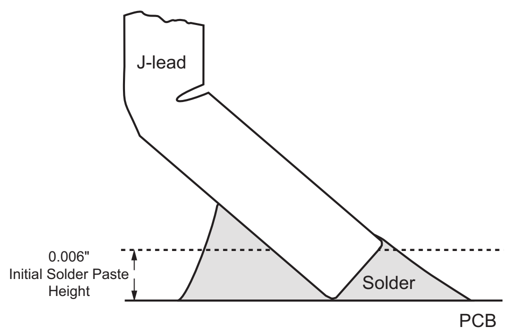


Figure 8 *(left):* *Example of a valid solder joint for a "long" J-lead with shallow bend (>20° angle)*

Figure 9 *(right):* *Example of an invalid solder joint for J-lead with shallow bend (>20° angle) and good coplanarity*



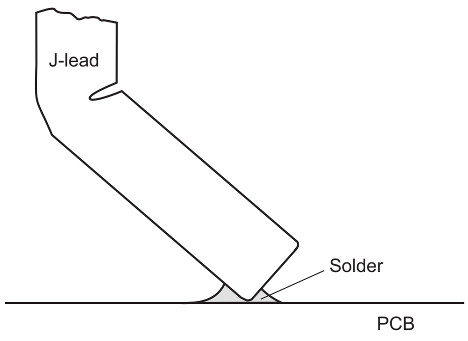
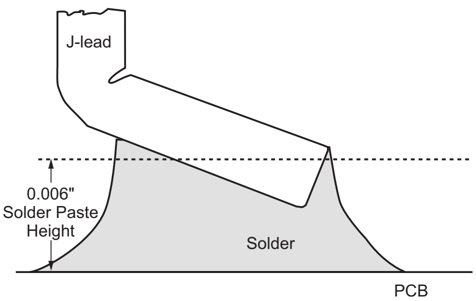


Figure 10 *(left):* *Example of a valid solder joint for a "short" J-lead with deep bend (<20° angle) and good coplanarity*

Figure 11 *(right):* *Example of an invalid solder joint for a "long" J-lead with deep bend (<20° angle) and good coplanarity*



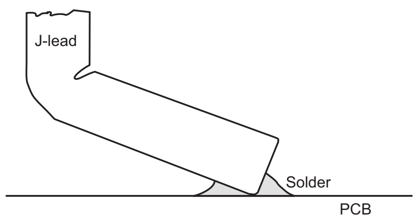
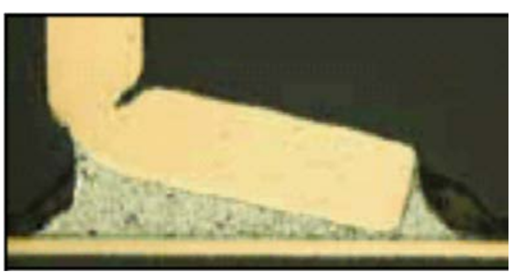
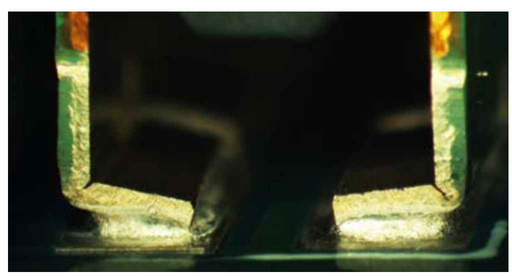


Figure 12 *(left):* *Cross-sectional view of an acceptable J-lead solder joint*

Figure 13 *(right):* *Acceptable J-lead solder joint (fillet under lead)*





The depth of this bond should extend the length of the J-lead. Note that only in corner cases, with good coplanarity and a J-lead with a close to 90° bend, does the solder joint resemble a traditional joint as defined in IPC-A-610 12.0 or other industry accepted criteria.

To address the topic of the blind solder joints, it is recommended that the process be carefully designed and tested such that the solder integrity of the inner row of J-leads can be guaranteed by design.

The reflowed solder joint itself should show evidence of proper wetting and conform to criteria set forth in IPC-A-610 or other industry standards accepted by the manufacturer or the solder used. An example of a properly wetted VI Chip module J-lead solder connection is shown in Figure 13.

Hand Soldering

J-lead VI Chip® modules are surface mount devices that are intended for attachment to a PCB via a convection reflow process. Hand soldering of VI Chip modules is not recommended for the following reasons:

1. The inner row of J-leads cannot be hand soldered and thus the VI Chip module cannot be completely attached to a printed circuit board.
2. A hand soldering iron is a point heat source that provides heating to reflow the solder joint in its immediate vicinity. The J-lead geometry, especially for power connections, is much longer than standard hand soldering tips, making it difficult to completely solder a single J-lead joint with a hand soldering iron.
3. The local heating of the soldering iron is prone to exceeding the peak temperature requirements in Table 2 unless it is set to a lower temperature, at which point it is often not hot enough to form a proper solder joint.

VI Chip Module Removal

VI Chip modules cannot be reused after removal from an application. If a VI Chip module needs to be replaced due to a manufacturing defect, failure, or other reason it is important to consider the following:

1. Is the reason for removal known and understood? There are numerous avenues which should be investigated before replacing the VI Chip module on the assembly. For example if the application is suspect, this should be investigated before replacement to prevent a recurring failure.
2. If a failure investigation is required, special care must be taken when removing the VI Chip module to preserve the failure site within the module for analysis.
3. Must the underlying PCB be preserved? If so, this may require extra steps that sacrifice the VI Chip module failure investigation in order to preserve the board.

To remove a VI Chip module use the following procedure:

1. The VI Chip module should be heated to >150°C using hot air and then pried up using a "lever" (such as a small screwdriver or tweezers).
2. If the temperature of the VI Chip module is below the melting point of the J-lead solder joint to the board, the VI Chip module will separate at the J-lead solder ball joint.
3. Residual belly glue on the board can be scraped off using a small screw driver while the temperature of the belly glue is kept above 150°C.

If the cause of failure must be investigated and/or the PCB does not need to be preserved, the VI Chip® modules can be removed by other means. The best way to preserve the failure site would be to submit the PCB (or card) containing the VI Chip module intact for Failure Analysis. Please note that the customer PCB will be destroyed in the process of analyzing the chip failure. If this is not feasible, mechanically separating the VI Chip module from the J-leads will preserve an internal electrical failure site, though once the body of the VI Chip module has been removed, the J-leads should be de-soldered from the PCB and included with the VI Chip module for complete FA. In general, heating the chip above 217°C during removal may destroy failure sites both internal to the VI Chip module and associated with the J-lead interface.

VI Chip Module Replacement, Printed Circuit Board Rework or Subsequent Wave Soldering after SMT Mounting

Dry baking of printed circuit board assemblies following VI Chip SMT mounting may be required depending on subsequent assembly processing needs and cumulative ambient environment exposure time. See MSL Handling section for full recommendations.

If a VI Chip component is to be removed from the customer printed circuit board, or a lead solder joint reworked, it is recommended that localized heating be used. Localized heating can limit the maximum body temperature of the VI Chips on the customer's printed circuit board to not to exceed 200°C. Minimizing the peak temperature of the VI Chip will minimize moisture related component damage. If the VI Chip body temperature cannot be maintained under 200°C, the entire printed circuit board must be baked dry for 48 hours at 125°C prior to rework and/or component removal per section 6.2 of the JEDEC standard J-STD-033C. VI Chip temperatures shall be measured at the top center of the package body.

This consideration for the VI Chip body temperature shall also be maintained during all subsequent wave soldering processes. During Wave soldering, the VI Chip body temperature shall not exceed 200°C as measured using a thermocouple on the top center of the package body. If the VI Chip body temperature cannot be maintained under 200°C during the wave soldering process, the entire printed circuit board must be baked dry for 48 hours at 125°C prior to wave soldering processing, ensuring that the top of the VI Chip reaches 125°C for 48 hours.

If a part next to the VI Chip is to be removed or reworked, the temperature of the VI Chip must be kept below 200°C during that rework process. If it is not possible to keep the VI Chip below 200°C, the entire printed circuit card board must be baked dry for 48 hours at 125°C prior to neighboring rework and/or component removal per section 6.2 of the JEDEC standard J-STD-033C. During this baking process, the VI Chip must be at 125°C for a minimum of 48 hours.

During reinstallation, replacement, rework of the VI Chip, reinstallation, replacement, rework of neighboring components to the VI Chip or subsequent wave soldering of the VI Chip, the package shall not exceed its MSL ratings per J-STD-020D.1 at any time during replacement or processing. Localized replacement reflow heating is recommended, so that the entire board is not re-subjected to reflow temperature profiles.

If during any reinstallation, replacement, rework, wave soldering of the, or next to, the VI Chip, the maximum temperature, as measured using a thermocouple on the top center of the package body, does not exceed 200°C, then dry baking, prior to processing, is not required.

Note: Temperatures on neighboring SMD packages above the melting point of the solder being used may cause some solder joints to partially reflow, which may result in a potential solder joint reliability concern.

Conclusion

The VI Chip® package presents a series of unique requirements when being reflow soldered onto a board. This document presents guidelines for MSL handling, reflow, post-reflow cleaning, and inspection of VI Chip modules. While every design and manufacturing process will be unique, using these guidelines when attaching VI Chip modules to a printed circuit board will minimize the risk of poor solder joints and failures due to improper soldering.

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