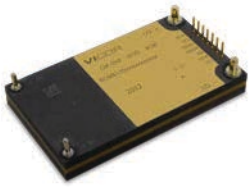
BCM® Bus Converter
BCM6135AJ2F5880A06



800V Input Automotive Ultra-High-Voltage Fixed-Ratio Bus Converter

Features & Benefits

- Up to 80A continuous low-voltage-side current
- 158.8kW/L typical power density
- 97.3% peak efficiency
- 4242V_{DC} input-to-output isolation
- Bidirectional start up and steady-state operation
- Parallel operation for multi-kW arrays
- OV, OC, UV, short-circuit and thermal fault monitoring
- PMBus® management interface
- Automotive APQP process + product development integration
- Integrated AECQ-100 qualified Vicor controller

Typical Applications

- Electric and Mild-Hybrid Vehicles
- Decentralized Architecture

Product Ratings				
Step-Down Operation	K = 1/16	V_{HI} = 800V (520 – 920V)	V_{LO} = 50V (32.5 – 57.5V) No Load	I_{LO} = 80A Max
Step-Up Operation		V_{LO} = 50V (32.5 – 57.5V)	V_{HI} = 800V (520 – 920V) No Load	I_{HI} = 5A Max

Product Description

The CM-ChiP BCM is a high-efficiency Bus Converter, operating from a 520 – 920V_{DC} high-voltage bus to create an isolated ratiometric 32.5 – 57.5V_{DC} low-side bus. This ultra-low-profile module is available in a board-mount form factor, incorporates a fixed-ratio DC-DC converter and PMBus commands and controls. The BCM provides low output impedance, low noise, fast transient response, high efficiency and high power density. A low-voltage-side-referenced PMBus-compatible telemetry and control interface provides access to the BCM's configuration, fault monitoring and other telemetry functions.

Owing to its megahertz bandwidth and low series impedance, the BCM performs as an efficient capacitance multiplier, enabling bulk capacitance across the low-voltage bus to be scaled down by a factor of 1/256 across the high-voltage bus. Capacitance multiplication cuts down the size and number of capacitors required by PoL regulators while freeing up real estate at the point-of-load.

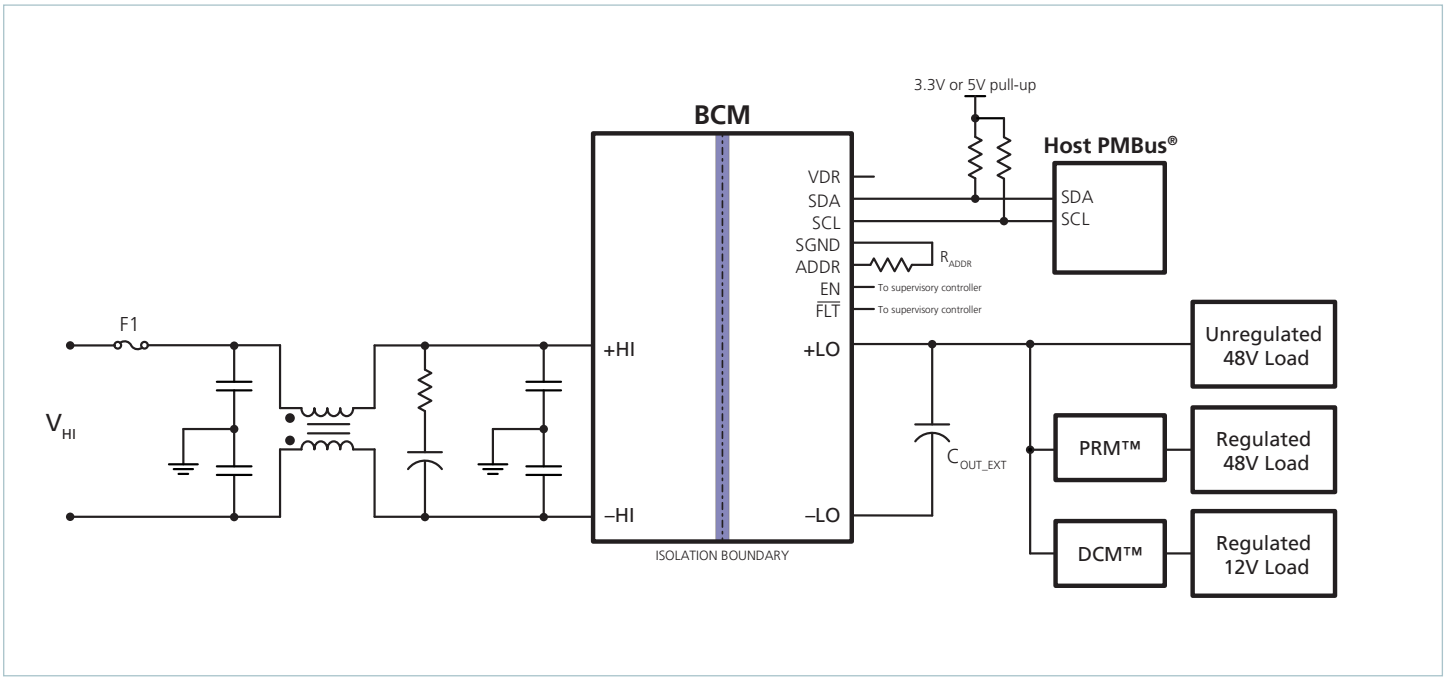
The CM-ChiP BCM module offers flexible thermal management options, with very low top- and bottom-side thermal impedances. Thermally-adept CM-ChiP-based power components enable customers to achieve low-cost power system solutions with previously unattainable system size, weight and efficiency attributes.

Package Information

- Through-Hole CM-ChiP™ Package
  2.42 x 1.39 x 0.29in
  [61.3 x 35.4 x 7.3mm]
- Weight: 58g

Note: Product images may not highlight current product markings and cosmetic features.

Typical Application



UHV BCM6135 CM-ChiP™ with PRM™ and DCM™

Terminal Configuration

Terminal Descriptions

Signal Name	Terminal Number	Terminal Functions
+HI	1	Positive High-Side: power terminal
–HI	2	Negative High-Side: power terminal
+LO	3	Positive Low-Side: power terminal
–LO	4	Negative Low-Side: power terminal
SDA	5	Digital serial communication data terminal
SCL	6	Digital serial communication clock terminal
SGND	7	Signal Ground: reference for address resistor (R_{ADDR}); do not reference other signals to SGND; keep SGND separated from –LO terminal in electrical design
ADDR	8	Digital serial communication address assignment
EN	9	Enable: when EN is asserted high, device is enabled
VDR	10	Factory use only
$\overline{FLT}$ [a]	11	$\overline{FLT}$ functions as a fault indicator; $\overline{FLT}$ is active low, and will pull low whenever the powertrain is faulted or disabled; configured as a push-pull output from the internal controller; driving this terminal will damage the module

[a] Overbar ($\overline{FLT}$) or star (FLT*) marking signify an active low designation.

Part Ordering Information

Part Number	Mounting Style	Product Grade	Tray Size
BCM6135**A**J2F5880**A**06	**A** = CM-ChiP™ Board Mount	**A** = Automotive	323 x 136 x 16mm 12 parts per tray Vicor PN 52948

Storage and Handling Information

Note: For compressive loading refer to Application Note AN:036, "Recommendations for Maximum Compressive Force of Heat Sinks."

Attribute	Comments	Specification
Storage Temperature Range		–40 to 125°C
Operating Internal Temperature Range	Temperature at the hottest internal component (T_{INT}) must not exceed this maximum	–40 to 125°C
Weight		58g
Package Plating		75µm copper with ENiG surface finish
ESD Rating	Human Body Model JEDEC JS-001-2023	Class 2 ≥2kV
	Charged Device Model JEDEC JS-002-2022	Class 2a ≥500V

Safety, Reliability and Agency Approvals

Attribute	Comments	Value	Unit
Dielectric Withstand	Input to output	4242	V_{DC}
	Input to case	4242	
	Output to case	1700	
Insulation Resistance	+HI to case	100	MΩ
	–HI to case	100	
MTTF	Telcordia SR-332 Issue 3, Method I Case 3, Ground Mobile	40.7	MHrs
FIT	Telcordia SR-332 Issue 3, Method I Case 3, Ground Mobile	24.6	FIT
Agency Approvals/Standards			
	UKCA, electrical equipment (safety) regulations		
	CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable		

Absolute Maximum Ratings

The ABSOLUTE MAXIMUM ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Operating beyond rated operating conditions for an extended period of time may affect device reliability. All voltages referenced to –LO unless otherwise noted. Positive terminal currents represent current flowing out of the terminal.

Parameter	Comments	Min	Max	Unit
Input Voltage (+HI to –HI)	Powertrain enabled	–5.1	960	V
	Powertrain disabled	–10.2	1000	
Output Voltage (+LO to –LO)		–1	60	V
SCL, SDA		–0.3	5.5	V
ADDR to SGND		–0.3	3.6	V
EN		–0.5	5.3	V
$\overline{FLT}$		–0.5	3.6	V

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted.
Boldface specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C and are assured to meet performance specification by design, test correlation, characterization and/or statistical process control. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Specifications						
Step-Down and Step-Up Operation						
Input Voltage Slew Rate	dV_{IN}/dt				**1**	V/µs
No-Load Power Dissipation	P_{NL}	EN high, V_{HI} = 800V or V_{LO} = 50V		23.4	**48**	W
Efficiency, Ambient	η_{AMB}	V_{HI} = 800V, I_{LO} = 50A, T_{CASE} = 25°C	96.74	97.29		%
		V_{HI} = 800V, I_{LO} = 25A, T_{CASE} = 25°C	96.72	97.44		
		V_{HI} = 520 – 920V, I_{LO} = min (smaller of 80A or 2500W/(V_{HI} • K)), T_{CASE} = 25°C	93			
Efficiency, Hot	η_{HOT}	V_{HI} = 800V, I_{LO} = 50A, T_{CASE} = 70°C	96	97.02		%
		V_{HI} = 800V, I_{LO} = 25A, T_{CASE} = 70°C	97	97.43		
		V_{HI} = 520 – 920V, I_{LO} = min (smaller of 80A or 2500W/(V_{HI} • K)), T_{CASE} = 70°C	91.5			
Switching Frequency	F_{SW}	Over rated line and load	**1.2**	**1.3**	**1.4**	MHz
Rated Output Power	P_{OUT_DC}	Continuous, V_{HI} = 520V or V_{LO} = 32.5V			**2500**	W
	P_{OUT_PEAK}	t_{PEAK} ≤ 20ms, 25% duty cycle, V_{HI} = 520V or V_{LO} = 32.5V			**3100**	W
Array Size	n_{ARRAY}				**7**	BCMs
Step-Down Operation						
High-Side Input Voltage Range	V_{HI}	Continuous, operating	**520**	800	**920**	V
Low-Side Output Voltage	V_{LO}	Continuous, operating; V_{LO} = V_{HI} • K – (I_{LO} • R_{LO})		50		V
Low-Side Output Voltage Ripple	V_{LO_PKPK}	V_{HI} = 520V, I_{LO} = 80A, C_{LO_EXT} = 0µF		0.4	0.5	V_{P-P}
		V_{HI} = 520V, I_{LO} = 80A, C_{LO_EXT} = 100µF		0.35	0.4	
		V_{HI} = 800V, I_{LO} = 50A, C_{LO_EXT} = 0µF		0.34	0.5	
		V_{HI} = 800V, I_{LO} = 50A, C_{LO_EXT} = 100µF		0.3	0.4	
Low-Side Output Current	I_{LO_DC}	Continuous, V_{HI} = 520V [b]			**80**	A
	I_{LO_PEAK}	t_{PEAK} ≤ 20ms, 25% duty cycle, V_{HI} = 520V [b]			**100**	
Low-Side Output Resistance	R_{LO}	V_{HI} = 800V, P_{LO} = 2500W		14.69	**30**	mΩ
High-Side Input Quiescent Current	I_{HI_Q}	EN low, V_{HI} = 800V		5.76	**8**	mA
High-Side OVLO Threshold Rising	V_{HI_OVLO+}		943		**960**	V
High-Side OVLO Hysteresis	$V_{HI\_OVLO\_HYS}$		23		25	V
Rated Low-Side Capacitance (External)	$C_{LO\_EXT\_SS}$	Rated capacitance for start up in a single soft-start cycle, see "Start Up (Step-Down Operation)" for details			100	µF
	C_{LO_EXT}	Rated capacitance for start up, see "Start Up (Step-Down Operation)" for details			1200	µF
	$C_{LO\_AEXT\_SS}$	Parallel array operation; $C_{LO\_AEXT\_SS}$ = N • 0.5 • $C_{LO\_EXT\_SS}$ max, where N = number of units parallel, rated capacitance for start up in a single soft-start cycle, see "Start Up (Step-Down Operation), Parallel Array Operation" for details				
	C_{LO_AEXT}	Parallel array operation; C_{LO_AEXT} = N • 0.5 • C_{LO_EXT} max, where N = number of units parallel, see "Start Up (Step-Down Operation), Parallel Array Operation" for details				

[b] See Figure 1 for the power de-rating curve depending on T_{CASE}.

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted.
Boldface specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C and are assured to meet performance specification by design, test correlation, characterization and/or statistical process control. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Specifications (Cont.)						
Step-Up Operation						
Low-Side Input Voltage Range	V_{LO}	Continuous, operating	**32.5**	50	**57.5**	V
High-Side Output Voltage	V_{HI}	Continuous, operating; $V_{HI} = (V_{LO} \bullet 1/K) - (I_{HI} \bullet R_{HI})$		800		V
High-Side Output Voltage Ripple	V_{HI_PKPK}	V_{LO} = 32.5V, I_{HI} = 5A, C_{HI_EXT} = 0nF		57	60	V_{P-P}
		V_{LO} = 50V, I_{HI} = 3.125A, C_{HI_EXT} = 0nF		37	40	
High-Side Output Current	I_{HI_DC}	Continuous, V_{LO} = 32.5V [b]			**5**	A
	I_{HI_PEAK}	t_{PEAK} ≤ 20ms, 25% duty cycle, V_{LO} = 32.5V [b]			**6.25**	
High-Side Output Resistance	R_{HI}	V_{LO} = 50V, P_{HI} = 2500W		6.58	**13**	Ω
Low-Side Input Quiescent Current	I_{LO_Q}	EN low, V_{LO} = 50V			**1**	µA
Low-Side OVLO Threshold Rising	V_{LO_OVLO+}		58		**60**	V
Low-Side OVLO Hysteresis	$V_{LO\_OVLO\_HYS}$		1.42		1.58	V
Rated High-Side Capacitance (External)	C_{HI_EXT}	Excessive capacitance will damage unit, see "Start Up (Step-Up Operation)" for details			0	nF
	C_{HI_AEXT}	Parallel array operation; excessive capacitance will damage unit, see "Start Up (Step-Up Operation)" for details			0	nF
Fault Detection and Response						
Auto Restart Time	$t_{AUTO\_RESTART}$	Start up into a persistent fault condition. Non-latching fault detection given $V_{HI} > V_{HI\_UVLO+}$ or $V_{LO} > V_{LO\_UVLO+}$	1.9	2	**2.1**	s
High-Side Voltage Initialization Threshold	$V_{HI\_CONTROL}$	High-side voltage where internal controller is initialized (powertrain inactive)	440	475	**520**	V
Low-Side Voltage Initialization Threshold	$V_{LO\_CONTROL}$	Low-side voltage where internal controller is initialized (powertrain inactive)	6	7	**32.5**	V
High-Side Undervoltage Threshold Rising	V_{HI_UVLO+}		480		**520**	V
High-Side Undervoltage Hysteresis	$V_{HI\_UVLO\_HYS}$		26		40	V
Low-Side Undervoltage Threshold Rising	V_{LO_UVLO+}		30.5		**32.5**	V
Low-Side Undervoltage Hysteresis	$V_{LO\_UVLO\_HYS}$		1.61		2.53	V
High-Side Undervoltage Start-Up Delay	$t_{HI\_LO\_DELAY}$		350	380	400	ms
Low-Side Undervoltage Start-Up Delay	$t_{LO\_HI\_DELAY}$		350	380	400	ms
Low-Side Overcurrent Shut Down	I_{LO_OC}			96	110	A
Low-Side Overcurrent Response Time	t_{LO_OC}				32	µs
Low-Side Short Circuit Shut Down	I_{LO_SHORT}			120	130	A
Low-Side Short Circuit Response Time	t_{LO_SHORT}				1	µs

[b] See Figure 1 for the power de-rating curve depending on T_{CASE}.

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted.
Boldface specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C and are assured to meet performance specification by design, test correlation, characterization and/or statistical process control. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
PMBus® Telemetry Characteristics						
READ_VIN Accuracy		From V_{HI} = 440 – 960V, across load	**–10**		**10**	%
READ_VIN Resolution				100		mV
READ_VIN Functional Range			**400**		**960**	V
READ_VOUT Accuracy		Across line and load	**–5**		**5**	%
READ_VOUT Resolution				10		mV
READ_VOUT Functional Range			**6**		**60**	V
READ_IOUT Accuracy		Across all line, >15A load	**–15**		**15**	%
READ_IOUT Resolution				10		mA
READ_IOUT Functional Range			**0**		**100**	A
READ_TEMPERATURE_1 Accuracy		Disabled, with T_{CASE} = 25°C	**–5**		**5**	°C
READ_TEMPERATURE_1 Resolution				**1**		°C
READ_TEMPERATURE_1 Functional Range			**–55**		**130**	°C
TON_DELAY Accuracy		Across all line and load	**–50**		**50**	µs
TON_DELAY Resolution				**1**		ms
TON_DELAY Functional Range			**0**		**100**	ms
OT_FAULT_LIMIT Accuracy		Across all line and load	**–5**		**5**	°C
OT_FAULT_LIMIT Resolution				**12.5**		°C
OT_FAULT_LIMIT Functional Range			**0**		**125**	°C
OT_WARN_LIMIT Accuracy		Across all line and load	**–5**		**5**	°C
OT_WARN_LIMIT Resolution				**12.5**		°C
OT_WARN_LIMIT Functional Range			**0**		**125**	°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (A-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Serial Clock: SCL Serial Data: SDA						
Serial Voltage Range	V_{SERIAL}		3.3		5	V
SCL Frequency	F_{SCL}		10		400	kHz
Input High Voltage	V_{IH}		2.3			V
Input Low Voltage	V_{IL}				1	V
Output High Voltage	V_{OH}		2.8			V
Output Low Voltage	V_{OL}				0.5	V
Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4		20	mA
Address: ADDR						
Address Registration Delay	t_{SADDR}			1		ms
Enable / Disable Control: EN						
Enable Current	I_{EN}	V_{EN} = 5V		1.61		mA
EN High Voltage	V_{EN_HIGH}		3.51			V
EN Low Voltage	V_{EN_LOW}				1.36	V
Output Turn-On Delay	t_{EN}	V_{HI_DC} > V_{HI_UVLO+}, EN high		2		ms
Fault: $\overline{FLT}$						
$\overline{FLT}$ Inactive Pull-Up Voltage	$V_{\overline{FLT}\_INACTIVE}$		2.8	3.3		V
Powertrain Active to $\overline{FLT}$ Time	$t_{\overline{FLT}}$	Powertrain active to $\overline{FLT}$ high		250		µs
$\overline{FLT}$ Active Sink Current	$I_{\overline{FLT}\_ACTIVE}$	Fault active, $V_{\overline{FLT}}$ = 400mV	4			mA

Specified Operating Area

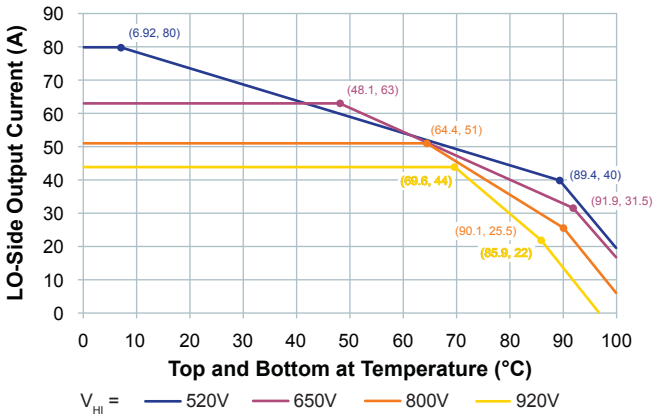


Figure 1 — *Specified thermal operating area: equal top and bottom surface temperatures at full rated output power*

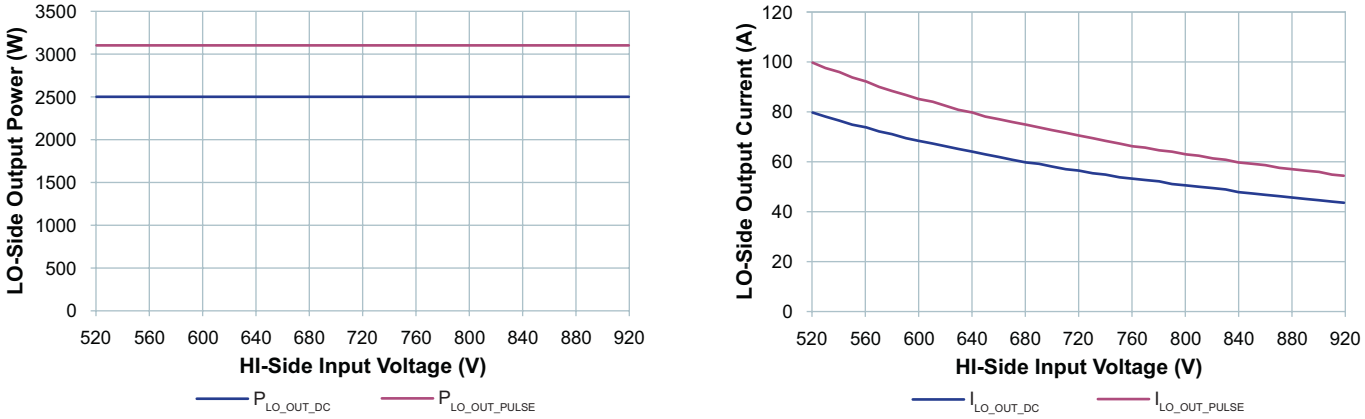


Figure 2 — *Specified electrical operating area using rated R_{LO}; T_{CASE} = 25°C*

Typical Performance Characteristics, Step-Down Operation

Temperature controlled via non-pin-side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the forward direction (high side to low side). See associated figures for general trend data.

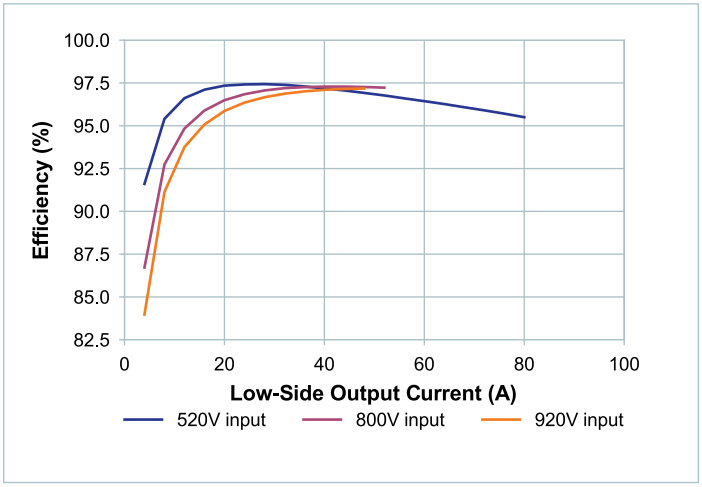


Figure 3 — *Efficiency at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = –40°C*

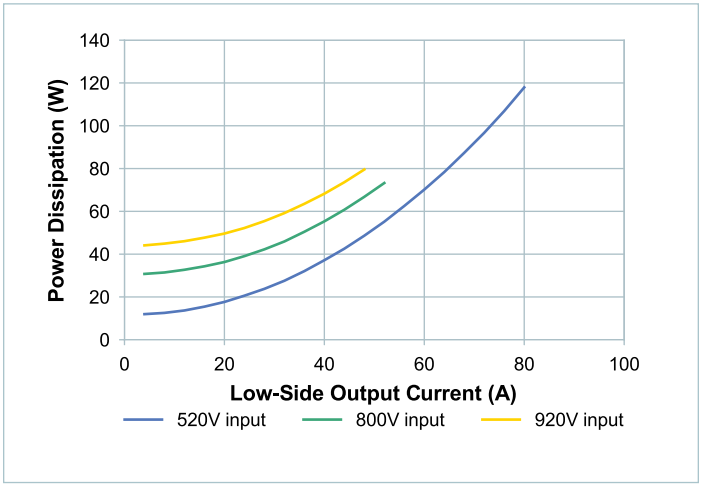


Figure 4 — *Power dissipation at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = –40°C*

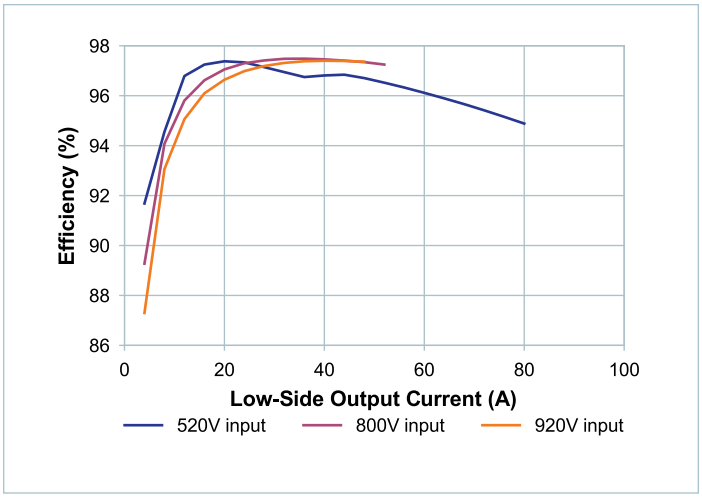


Figure 5 — *Efficiency at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = 25°C*

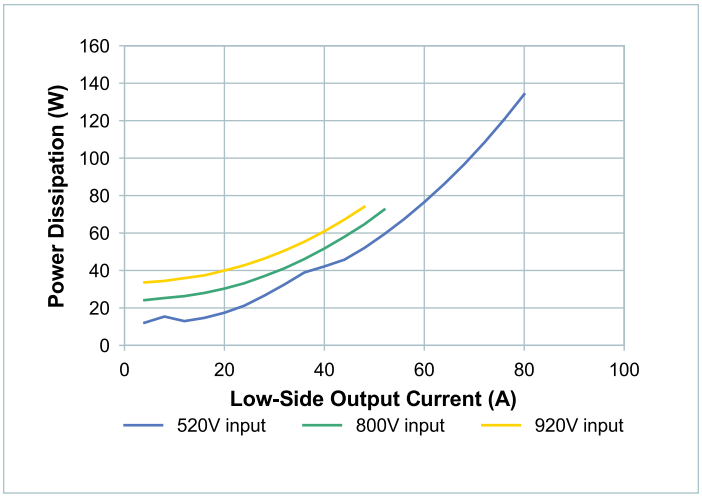


Figure 6 — *Power dissipation at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = 25°C*

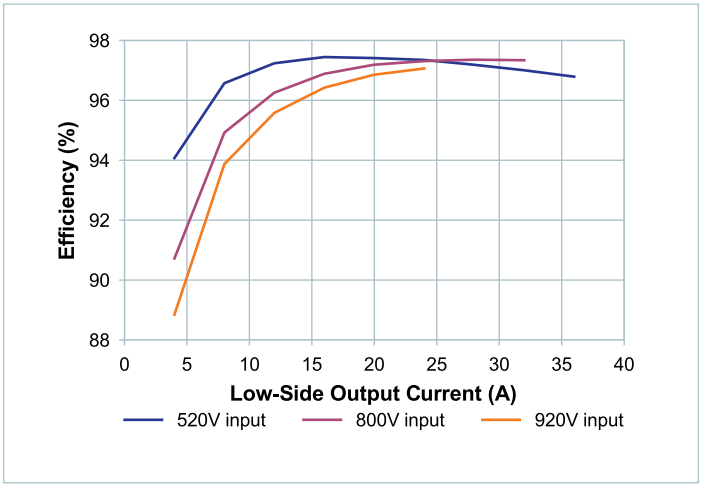


Figure 7 — *Efficiency at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = 100°C*

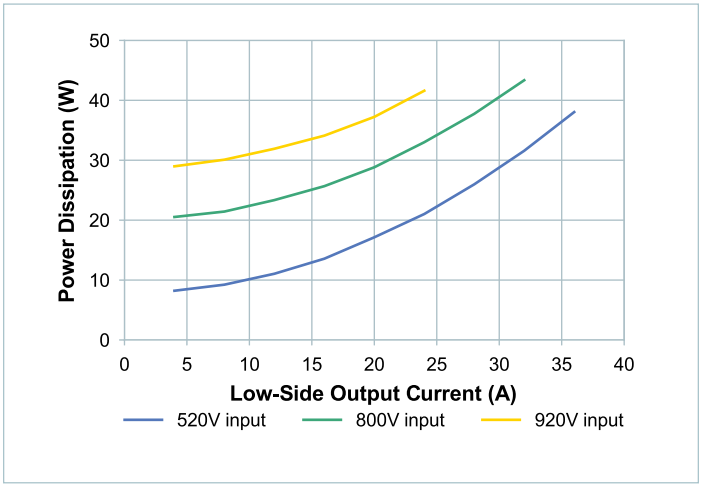


Figure 8 — *Power dissipation at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = 100°C*

Typical Performance Characteristics, Step-Up Operation

Temperature controlled via non-pin-side cold plate, unless otherwise noted. All data presented in this section are collected from units processing power in the reverse direction (low side to high side). See associated figures for general trend data.

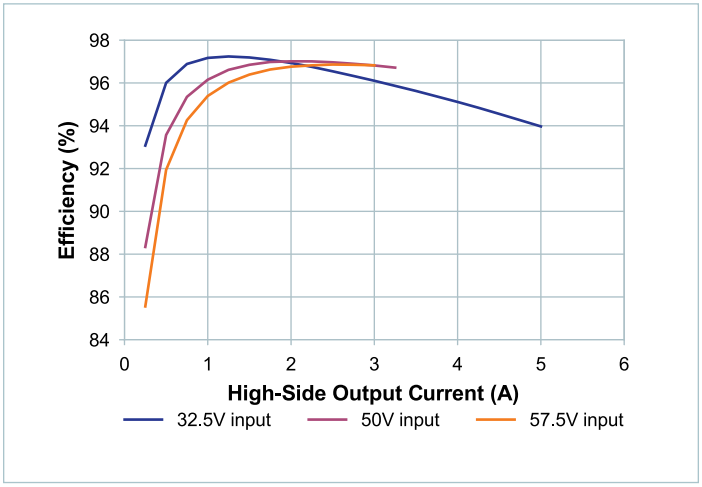


Figure 9 — *Efficiency at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = –40°C*

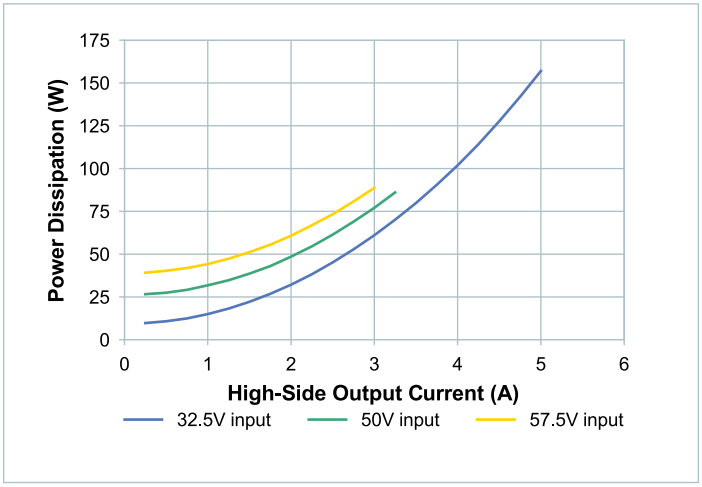


Figure 10 — *Power dissipation at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = –40°C*

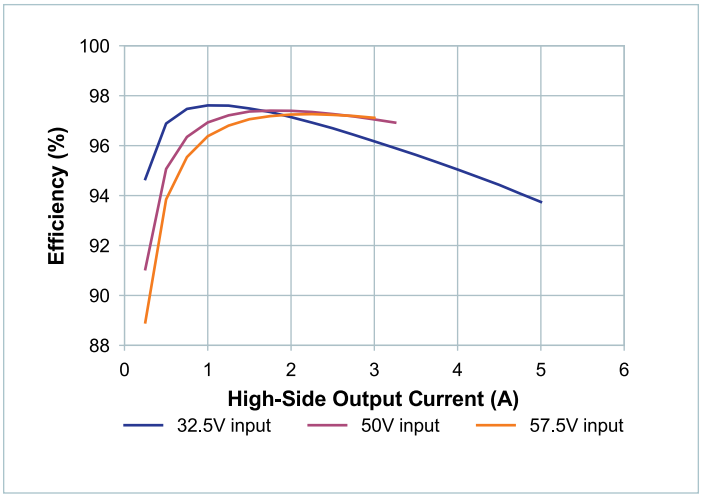


Figure 11 — *Efficiency at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = 25°C*

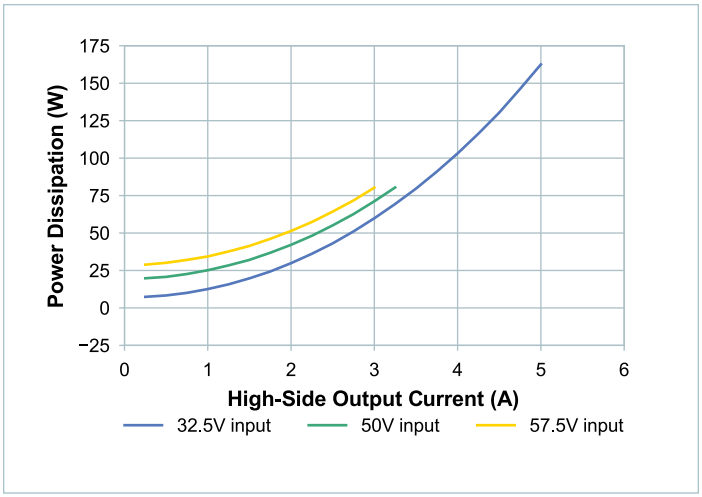


Figure 12 — *Power dissipation at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = 25°C*

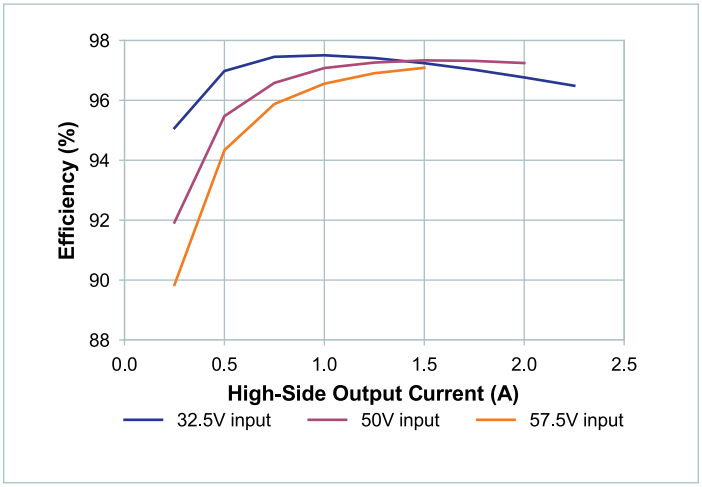


Figure 13 — *Efficiency at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = 100°C*

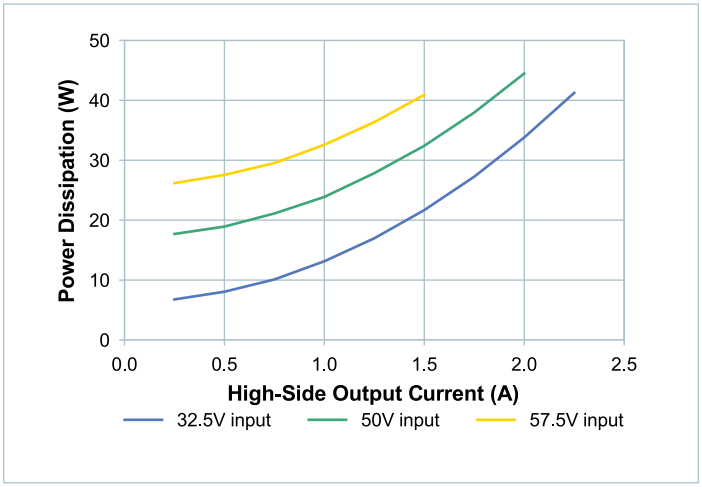


Figure 14 — *Power dissipation at $T_{NON\text{-}PIN\_SIDE}$, T_{PIN_SIDE} = 100°C*

Typical Performance Characteristics, No-Load Operation

Temperature controlled via non-pin-side cold plate, unless otherwise noted. See associated figures for general trend data.

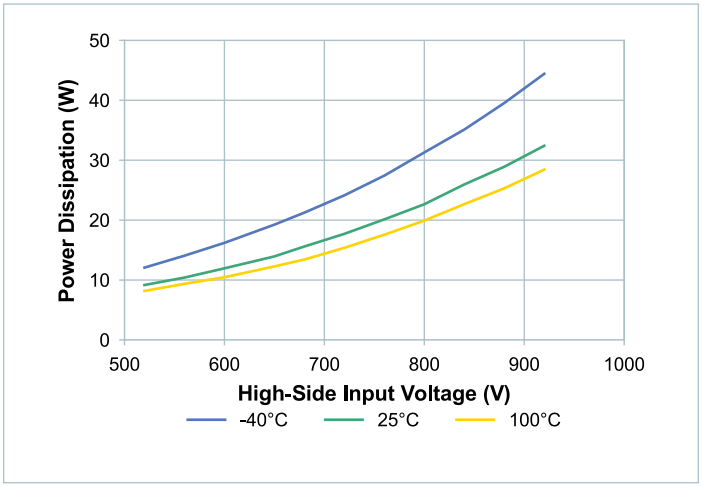


Figure 15 — *No-load power dissipation vs. V_{HI}*

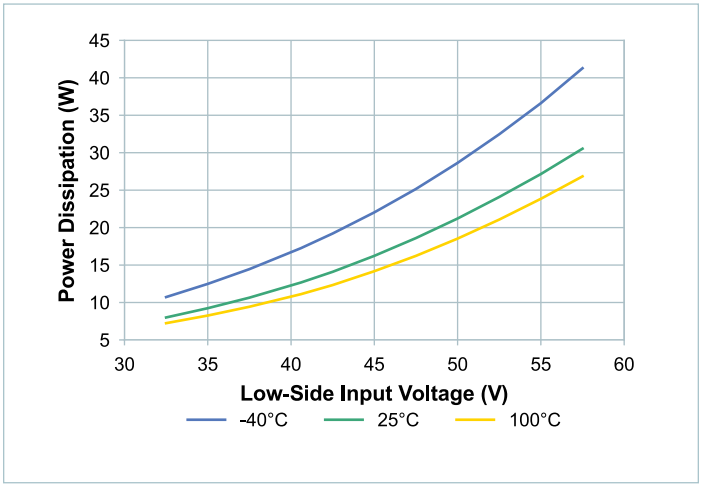
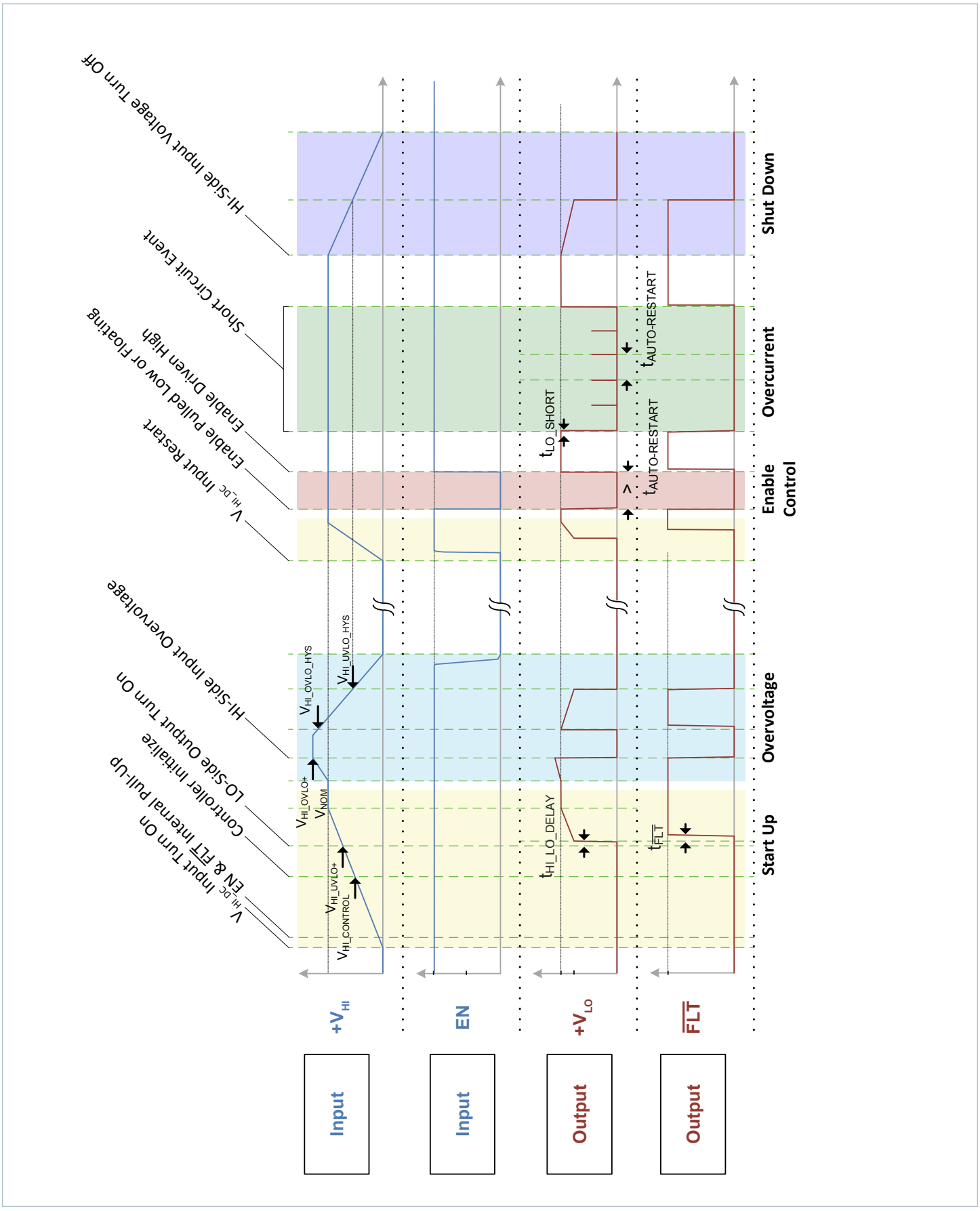


Figure 16 — *No-load power dissipation vs. V_{LO}*

Timing Diagram (Forward Direction)



BCM in a CM-ChiP™

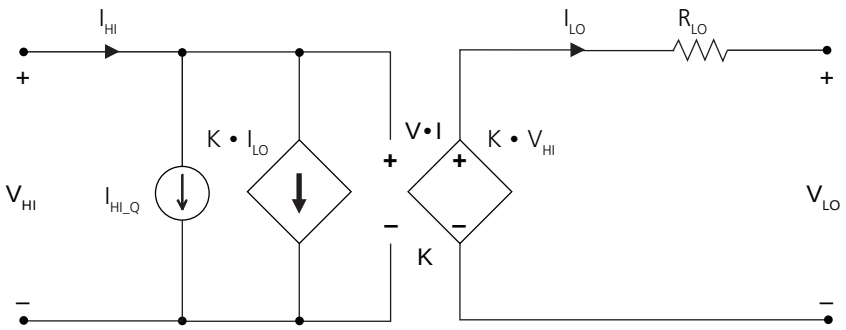


Figure 17 — *BCM DC model*

The BCM uses a high-frequency resonant tank to move energy from the high-voltage side to low-voltage side and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of the high-side voltage and the low-side current. A small amount of capacitance embedded in the high-voltage-side and low-voltage stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM6135 can be simplified into the model shown in Figure 17.

At no load:

$$V_{LO} = V_{HI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the BCM.
Rearranging Equation 1:

$$K = \frac{V_{LO}}{V_{HI}} \qquad (2)$$

In the presence of a load, V_{LO} is represented by:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R_{LO} \qquad (3)$$

and I_{LO} is represented by:

$$I_{LO} = \frac{I_{HI} - I_{HI\_Q}}{K} \qquad (4)$$

R_{LO} represents the impedance of the BCM, and is a function of the R_{DS_ON} of the high-voltage-side and low-voltage-side MOSFETs and the winding resistance of the power transformer. I_{HI_Q} represents the quiescent current of the BCM controller, gate drive circuitry and core losses.

The effective DC voltage transformer action provides additional interesting attributes. Assuming that R_{LO} = 0Ω and I_{HI_Q} = 0A, Equation 3 now becomes Equation 1 and is essentially load independent, resistor R is now placed in series with V_{HI}.

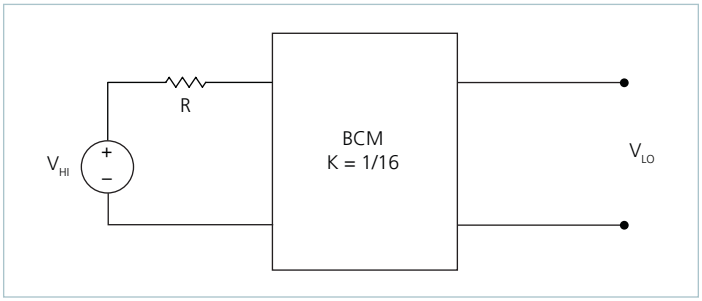


Figure 18 — *K = 1/16 BCM with series high-voltage-side resistor*

The relationship between V_{HI} and V_{LO} becomes:

$$V_{LO} = \left(V_{HI} - I_{HI} \bullet R\right) \bullet K \qquad (5)$$

Substituting the simplified version of Equation 4 (I_{HI_Q} is assumed = 0A) into Equation 5 yields:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Equation 3, where R_{LO} is used to represent the characteristic impedance of the BCM. However, in this case a real resistor, R on the high-voltage side of the BCM is effectively scaled by K^2 with respect to the low-voltage side.

Assuming that R = 1Ω, the effective R as seen from the low-voltage side is 3.9mΩ, with K = 1/16.

A similar exercise can be performed with the additon of a capacitor or shunt impedance at the high-voltage side of the BCM. A switch in series with V_{HI} is added to the circuit. This is depicted in Figure 19.

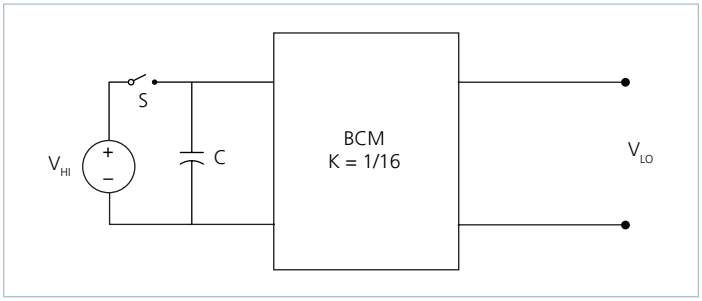


Figure 19 — *BCM with high-voltage-side capacitor*

A change in V_{HI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{HI}}{dt} \quad (7)$$

Assume that with the capacitor charged to V_{HI}, the switch is opened and the capacitor is discharged through the idealized BCM. In this case,

$$I_C = I_{LO} \bullet K \quad (8)$$

substituting Equation 1 and 8 into Equation 7 reveals:

$$I_{LO}(t) = \frac{C}{K^2} \bullet \frac{dV_{LO}}{dt} \quad (9)$$

The equation in terms of the low-voltage side has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the low-voltage side when expressed in terms of the high-voltage side. With K = 1/16 as shown in Figure 19, C = 0.39µF would appear as C = 100µF when viewed from the low-voltage side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a BCM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, these benefits are not achieved if the series impedance of the BCM is too high. The impedance of the BCM must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the BCM low involves switching at a high frequency. This enables the use of small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low-loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM are:

- No load power dissipation (P_{HI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{LO}}$): refers to the power loss across the BCM modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{HI\_NL} + P_{R_{LO}} \quad (10)$$

Therefore,

$$P_{LO\_OUT} = P_{HI\_IN} - P_{DISSIPATED} = P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{LO\_OUT}}{P_{HI\_IN}} = \frac{P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}}}{P_{HI\_IN}} \quad (12)$$

$$= \frac{V_{HI} \bullet I_{HI} - P_{HI\_NL} - (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}$$

$$= 1 - \left(\frac{P_{HI\_NL} + (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}\right)$$

Input and Output Filter Design

A major advantage of BCM systems versus conventional PWM converters is that the transformer based BCM does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of high-voltage-side voltage and low-voltage-side current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the high-voltage-side and low-voltage-side stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- *Guarantee low source impedance:*

  To take full advantage of the BCM's dynamic response, the impedance presented to its high-voltage-side terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- *Further reduce high-voltage-side and/or low-voltage-side voltage ripple without sacrificing dynamic response:*

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the high-voltage-side source will appear at the low-voltage side of the module multiplied by its K factor.

- *Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:*

  The module high- and low-voltage-side voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating high-voltage-side range. Even when disabled, the powertrain is exposed to the applied voltage and the power MOSFETs must withstand it.

Owing to the wide bandwidth and minimal low-voltage-side impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the high-voltage side of the module. At frequencies <500kHz the module appears as an impedance of R_{LO} between the source and load.

Within this frequency range, capacitance at the high-voltage side appears as effective capacitance on the low-voltage side per the relationship defined in Equation 13.

$$C_{LO} = \frac{C_{HI}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Start Up (Step-Down Operation)

Non-capacitive loading of the BCM must be delayed until the completion of soft-start. The $\overline{FLT}$ signal terminal voltage can used to determine when soft-start has successfully completed and the load can be safely enabled. A load must not be present on the low-side if the powertrain is not actively switching and high-side voltage is present.

Single-Module Operation

If a capacitive load greater than $C_{LO\_EXT\_SS}$ is present on the low-side and no precharge voltage or a precharge voltage less than $V_{LO\_PRECHARGE}$ is applied, the BCM will register the capacitor inrush current as an overcurrent event and shutdown. Once $t_{AUTO\_RESTART}$ expires the BCM will attempt to start again. During these restart periods a small amount/pulse of energy will be transferred from the high-side to the low-side. This energy transfer allows for the BCM to charge an external capacitor value up to C_{LO_EXT}.

Depending on the value of C_{LO_EXT}; the voltage applied to high-side of the BCM; and the voltage applied to the low-side of the BCM, the time required to complete soft-start will be in the range of 2.5 to 12 seconds.

In order for the BCM to start in the same amount of time as $C_{LO\_EXT\_SS}$ with a capacitance greater than $C_{LO\_EXT\_SS}$, a precharge voltage must be applied.

Equation 14 can be used to determine the minimum precharge voltage required to start the BCM in a single soft-start cycle with a capacitance greater than $C_{LO\_EXT\_SS}$:

$$V_{LO\_PRECHARGE} = \frac{V_{HI}}{16} - 4V \qquad (14)$$

Failure to follow these guidelines will result in the BCM never completing soft-start and the unit will fail to turn on. This will continue until power is removed.

Parallel Array Operation

If a capacitive load greater than $C_{LO\_AEXT\_SS}$ is present on the low-side and no precharge voltage or a precharge voltage less than $V_{LO\_PRECHARGE}$ is applied, the BCM(s) will register the capacitor inrush current as an overcurrent event and shut down.
Once $t_{AUTO\_RESTART}$ expires the BCM(s) will attempt to start again. During these restart periods a small amount/pulse of energy will be transferred from the high-side to the low-side. This energy transfer allows for the BCM to charge an external capacitor value up to C_{LO_AEXT}.

The maximum capacitance value that an array of n BCMs can start up in a single soft-start cycle can be derived from the following equation:

$$C_{LO\_AEXT\_SS} = N \bullet 0.5 \bullet C_{LO\_EXT\_SS}\,(max) \qquad (15)$$

The maximum capacitance value that an array of n BCMs can start up into can be derived from the following equation:

$$C_{LO\_AEXT} = N \bullet 0.5 \bullet C_{LO\_EXT}\,(max) \qquad (16)$$

Depending on the value of C_{LO_AEXT}; the voltage applied to high side of the BCM; and the voltage applied to the low-side of the BCM, the time required to complete soft-start will be in the range of 2.5 to 12 seconds.

In order for the BCM to start in the same amount of time as $C_{LO\_AEXT\_SS}$ with a capacitance greater than $C_{LO\_AEXT\_SS}$, a precharge voltage must be applied.

Equation 14 can be used to determine the minimum precharge voltage required to start the BCM in a single soft-start cycle with a capacitance greater than $C_{LO\_AEXT\_SS}$.

Failure to follow these guidelines will result in the BCMs never completing soft start and the units will fail to turn on. This will continue until power is removed.

Start Up (Step-Up Operation)

BCMs are capable of reverse power operation. Any loading of the BCM must be delayed until the completion of soft-start regardless of the load type. Once the unit is started, energy will be transferred from the low-voltage side back to the high-voltage side whenever the low-voltage-side voltage exceeds V_{HI} • K. The module will continue operation in this fashion for as long as no faults occur. Any energy storage applied to the low-side may result in unintentional reverse power operation if V_{HI} is less than V_{LO} • 1/K.

The $\overline{FLT}$ signal terminal voltage can used to determine when soft-start has successfully completed and the load can be safely enabled. A load must not be present on the high-side if the powertrain is not actively switching and low-side voltage is present.

In order to avoid damaging the BCM a precharge voltage must be applied if the capacitance applied to the high-side terminals of the BCM is greater than C_{HI_EXT}.

The following equation can be used to determine the minimum precharge voltage required to start the BCM in safely with a capacitance greater than C_{HI_EXT} or C_{HI_AEXT}:

$$V_{HI\_PRECHARGE} = (V_{LO} \bullet 16) - 4V \qquad (17)$$

If a fault occurs when in step-up operation an external circuit is required to guarantee that the pre-charge voltage is applied before the BCM restarts after $t_{AUTO\_RESTART}$ expires or attempting to manually restart the BCM.

BCM high-side short circuit events will result in damage to the powertrain of the BCM.

These restrictions apply to both a single BCM in step-up operation, as well as an array of BCMs in step-up operation.

Current Sharing

The performance of the BCM topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCMs of a given part number are connected in an array, they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load. Ensuring equal current sharing among modules requires that BCM array impedances be matched.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- A dedicated input filter for each BCM in an array is required to prevent circulating currents.

For further details see:
AN:016 Using BCM Bus Converters in High Power Arrays.

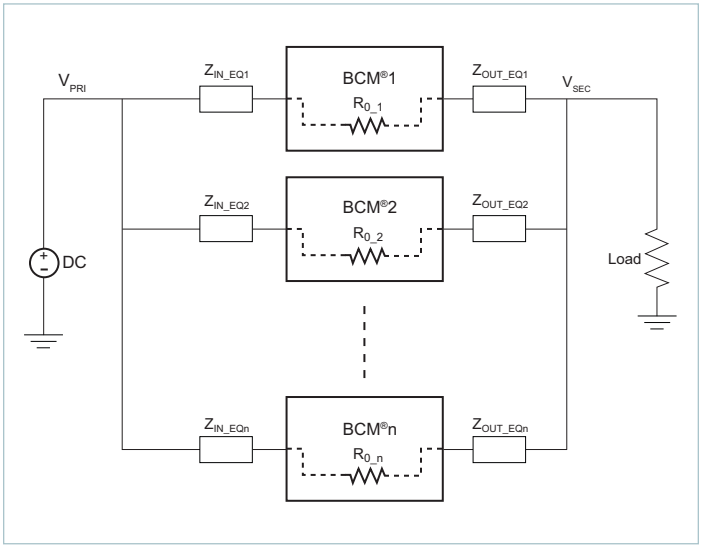


Figure 20 — *BCM parallel array*

Fuse Selection

In order to provide flexibility in configuring power systems, CM-ChiP™ modules are not internally fused. Input line fusing of CM-ChiP products is recommended at the system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of BCM)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: See safety agency approvals.

Reverse Operation

BCMs are capable of reverse power operation. Once the unit is started, energy will be transferred from the low-voltage side back to the high-voltage side whenever the low-voltage-side voltage exceeds $V_{HI} \bullet K$. The module will continue operation in this fashion for as long as no faults occur.

Transient operation in reverse is expected in cases where there is significant energy storage on the output and transient voltages appear on the input.

Fault Handling

HI-Side Undervoltage

Module Behavior

The HI-side undervoltage status is checked when the module EN terminal is asserted in the active state, prior to powertrain start up from the HI-side input. If the HI-side voltage is below the HI-side undervoltage threshold rising (V_{HI_UVLO+}) by more than the undervoltage hysteresis ($V_{HI\_UVLO\_HYS}$) at the time the EN terminal is asserted, the converter recognizes a fault condition and is prevented from starting up. Once the HI-Side UVLO fault is detected by the fault protection logic, the converter waits for the HI-side voltage to rise above the V_{HI_UVLO+} threshold. Provided the unit's EN terminal is still held in the active state, the module will start automatically.

The $\overline{FLT}$ terminal will be logic-low during a HI-side UVLO condition.

PMBus Reporting Characteristics

A HI-side UVLO condition is registered by the PMBus® telemetry and reporting interface. In STATUS_BYTE (78h), the VIN_UV_FAULT bit is asserted. In the high byte of STATUS_WORD (79h), the INPUT FAULT OR WARNING bit is asserted. In STATUS_INPUT (7Ch), the VIN_UV_FAULT bit is asserted.

All fault flags, if set, will remain asserted until cleared by the user or once the module's internal bias generation is disabled by $V_{HI\_DC} < V_{HI\_CONTROL}$ or $V_{LO\_DC} < V_{LO\_CONTROL}$.

HI-Side Overvoltage

Module Behavior

The HI-side overvoltage status is checked when the module EN terminal is asserted in the active state, prior to powertrain start up from the HI-side input. If the HI-side voltage is above the V_{HI_OVLO+} threshold at the time the EN terminal is asserted, the converter recognizes a fault condition and is prevented from starting up. After an OVLO fault occurs, the converter will wait for the HI-side voltage to fall below the HI-side overvoltage threshold rising (V_{HI_OVLO+}) by more than the HI-side overvoltage hysteresis ($V_{HI\_OVLO\_HYS}$). Provided the unit's EN terminal is still held in the active state, the module will start automatically.

The $\overline{FLT}$ terminal will be logic-low during a HI-side OVLO condition.

PMBus Reporting Characteristics

A HI-Side OVLO condition is registered by the PMBus telemetry and reporting interface. In the high byte of STATUS_WORD (79h), the INPUT FAULT OR WARNING bit is asserted. In STATUS_INPUT (7Ch), the VIN_OV_FAULT bit is asserted.

All fault flags, if set, will remain asserted until cleared by the user or once the module's internal bias generation is disabled by $V_{HI\_DC} < V_{HI\_CONTROL}$ or $V_{LO\_DC} < V_{LO\_CONTROL}$.

LO-Side Undervoltage

Module Behavior

The LO-side undervoltage status is checked when the module EN terminal is asserted in the active state, prior to powertrain start up from the LO-side input. If the LO-side voltage is below the LO-side undervoltage threshold rising (V_{LO_UVLO+}) by more than the LO-side undervoltage hysteresis ($V_{LO\_UVLO\_HYS}$) at the time the EN terminal is asserted, the converter recognizes a fault condition and is prevented from starting up. Once the LO-side UVLO fault is detected by the fault protection logic, the converter waits for the LO-side voltage to rise above the V_{LO_UVLO+} threshold. Provided the unit's EN terminal is still held in the active state, the module will start automatically.

If the converter is running and the LO-side voltage falls below $V_{LO\_UVLO\_HYS}$ threshold during powertrain operation, the converter recognizes a fault condition, the powertrain stops switching, and the LO-side output of the unit falls. Once the UVLO fault is detected by the fault protection logic, the converter shuts down and waits for the LO-side voltage to rise above the V_{LO_UVLO+} threshold. Provided the unit's EN terminal is not held in the inactive state, the module will restart automatically.

The $\overline{FLT}$ terminal will be logic-low during a UVLO condition.

PMBus Reporting Characteristics

A LO-side UVLO condition is registered by the PMBus® telemetry and reporting interface. In the high byte of STATUS_WORD (79h), the VOUT FAULT OR WARNING bit is asserted. In STATUS_VOUT (7Ah), the VOUT_UV_FAULT bit is asserted.

All fault flags, if set, will remain asserted until cleared by the user or once the module's internal bias generation is disabled by $V_{HI\_DC} < V_{HI\_CONTROL}$ or $V_{LO\_DC} < V_{LO\_CONTROL}$.

LO-Side Overvoltage

Module Behavior

The LO-side overvoltage status is checked when the module EN terminal is asserted in the active state, prior to powertrain start up from the LO-side input. If the LO-side voltage is above the $V_{LO\text{-}OVLO+}$ threshold at the time the EN terminal is asserted, the converter recognizes a fault condition and is prevented from starting up. After an OVLO fault occurs, the converter will wait for the LO side voltage to fall below the LO-side overvoltage threshold rising (V_{LO_OVLO+}) by at least the LO-side overvoltage hysteresis ($V_{LO\_OVLO\_HYS}$). Provided the unit's EN terminal is still held in the active state, the module will start automatically.

When the LO-side voltage is higher than the $V_{LO\text{-}OVLO+}$ threshold during powertrain operation, an OVLO fault is detected, the powertrain stops switching, and the LO-side output of the unit falls. Once the OVLO fault is detected by the fault protection logic, the converter shuts down and waits for the LO-side voltage to fall below the LO-side overvoltage threshold rising (V_{LO_OVLO+}) by at least the LO-side overvoltage hysteresis ($V_{LO\_OVLO\_HYS}$). Provided the unit's EN terminal is not held in the inactive state, the module will restart automatically.

The $\overline{FLT}$ terminal will be logic-low during an OVLO condition.

PMBus Reporting Characteristics

An OVLO condition is registered by the PMBus telemetry and reporting interface. In STATUS_BYTE (78h), the VOUT_OV_FAULT bit is asserted. In the high byte of STATUS_WORD (79h), the VOUT FAULT OR WARNING bit is asserted. In STATUS_VOUT (7Ah), the VOUT_OV_FAULT bit is asserted.

All fault flags, if set, will remain asserted until cleared by the user or once the module's internal bias generation is disabled by $V_{HI\_DC} < V_{HI\_CONTROL}$ or $V_{LO\_DC} < V_{LO\_CONTROL}$.

LO-Side Output Overcurrent

Module Behavior

When the LO side output current of the unit exceeds the LO side overcurrent trip threshold, an overcurrent fault is detected, the powertrain stops switching, and the LO-side output of the unit falls. The unit will automatically try to restart according to a defined $t_{AUTO\_RESTART}$ until the overcurrent condition is removed and normal operation resumes.

The $\overline{FLT}$ terminal will be logic-low during an overcurrent fault condition. Upon removal of the overcurrent condition and completion of soft-start, the $\overline{FLT}$ terminal will be asserted high.

PMBus Reporting Characteristics

An overcurrent condition is registered by the PMBus telemetry and reporting interface. In STATUS_BYTE (78h), the IOUT_OC_FAULT bit is asserted. In STATUS_IOUT (7Bh), the IOUT_OC_FAULT bit is asserted. In STATUS_MFR_SPECIFIC (80h), the VTM_OCS_FAULT bit is asserted.

All fault flags, if set, will remain asserted until cleared by the host or once the BCM HI-side input power is removed.

LO-Side Output Short Circuit

Module Behavior

When the LO-side output current of the unit exceeds the LO-side short-circuit trip threshold, an overcurrent fault is detected, the powertrain stops switching, and the LO-side output of the unit falls. The unit will automatically try to restart according to a defined $t_{AUTO\_RESTART}$ until the short circuit condition is removed and normal operation resumes.

The $\overline{FLT}$ terminal will be logic-low during a short circuit fault condition. Upon removal of the short circuit condition and completion of soft start, the $\overline{FLT}$ terminal will be asserted high.

PMBus Reporting Characteristics

A short circuit condition is registered by the PMBus telemetry and reporting interface. In STATUS_BYTE (78h), the IOUT_OC_FAULT bit is asserted. In STATUS_IOUT (7Bh), the IOUT_OC_FAULT bit is asserted. In STATUS_MFR_SPECIFIC (80h), the VTM_OCF_FAULT bit is asserted.

All fault flags, if set, will remain asserted until cleared by the host or once the BCM HI-side input power is removed.

Soft-Start Ramp Fault

Module Behavior

An overload condition during soft start is monitored by the powertrain. Should the LO-side output voltage fail to reach steady state prior to the end of the soft-start timer, a start-up overload or start-up short circuit fault is registered, the powertrain stops switching, and LO-side output of the unit falls. Provided the unit's EN terminal is not held in the inactive state, the module will attempt to restart according to a defined $t_{AUTO\_RESTART}$ until the overload or short circuit condition is removed.

The $\overline{FLT}$ terminal will be asserted low during the soft-start sequence as an indication to downstream connected power modules and/or loads that their operation should be held off until the completion of BCM soft start.

PMBus Reporting Characteristics

A soft-start ramp fault is registered by the PMBus telemetry and reporting interface. In STATUS_MFR_SPECIFIC (80h), the VTM_SS_TOUT_FAULT bit will be asserted.

All fault flags, if set, will remain asserted until cleared by the host or once the BCM HI-side or LO-side input power is removed.

Overtemperature

Module Behavior

The BCM features a thermal shut down, T_{OT}, which is designed to protect against catastrophic failure due to excessive temperatures. The overtemperature shut down cannot be used to ensure the device stays within the recommended operating temperature range, because it engages when the product is operated above the maximum rated temperature. As with other fault protections, when overtemperature shut down occurs, the BCM stops processing power and $\overline{FLT}$ drives low. Provided the converter's EN terminal is not held in the inactive state, the BCM will restart after the temperature has decreased.

The $\overline{FLT}$ terminal will be logic-low during an overtemperature fault condition. Upon return of the module to safe operating temperatures and completion of soft start, the $\overline{FLT}$ terminal will be asserted high.

PMBus Reporting Characteristics

An overtemperature fault is registered by the PMBus telemetry and reporting interface. In STATUS_BYTE (78h), the TEMPERATURE FAULT OR WARNING bit is asserted. In STATUS_TEMPERATURE (7Dh), the OT_FAULT bit is asserted.

The default overtemperature shut down threshold is 125°C. The user may configure the overtemperature shutdown threshold from 0 – 100% of the rated 125°C max through the OT_FAULT_LIMIT (4Fh) command.

The module's temperature monitoring is also used to warn the user of a high-temperature operating condition via the OT_WARNING bit in STATUS_TEMPERATURE (7Dh). A monitored temperature exceeding a user-defined threshold asserts the OT_WARNING bit. The user may set an warning threshold from 0 – 100% of the 125°C maximum internal operating temperature through the OT_WARN_LIMIT (51h) command. The default warning threshold is 100%.

All fault and warning flags, if set, will remain asserted until cleared by the host or once the BCM HI-side input power is removed.

Thermal Considerations

The CM-ChiP™ module provides a high degree of flexibility in that it presents several pathways to remove heat from the internal power dissipating components. Heat may be removed from the non-pin side and pin-side surfaces of the package as well as the power and signal pins. The extent to which these surfaces are cooled is a key component in determining the maximum power that is available from a CM-ChiP.

Module Maximum Internal Temperature

Since the CM-ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. Given that there are multiple pathways to remove heat from the CM-ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal temperatures are represented as voltage sources and the thermal resistances are represented as resistors.

Figure 8 shows the "thermal circuit" for a BCM6135 CM-ChiP in a two-sided cooling application, where the product is cooled through a heat sink at the pin side and a separate heat sink at the non-pin side. In this case, the BCM non-pin side and pin side (each heat sink) surface temperatures are represented as $T_{NON-PIN\_SIDE}$ and T_{PIN_SIDE}. This thermal system can now be very easily analyzed as an electrical network with simple resistors, voltage sources and a current source. The results of the simulation provide an estimate of heat flow through the various dissipation pathways as well as internal temperature.

PMBus Temperature Reporting

The PMBus® command READ_TEMPERATURE_1 (8Dh) returns the internally monitored junction temperature of the controller IC. READ_TEMPERATURE_1 is not sufficient to design or validate any module level thermal solution. Correct thermal design must use the module power dissipation and the module thermal resistance model given in Figure 8 to ensure that all areas of the module internal circuitry are kept below the maximum operating temperature.

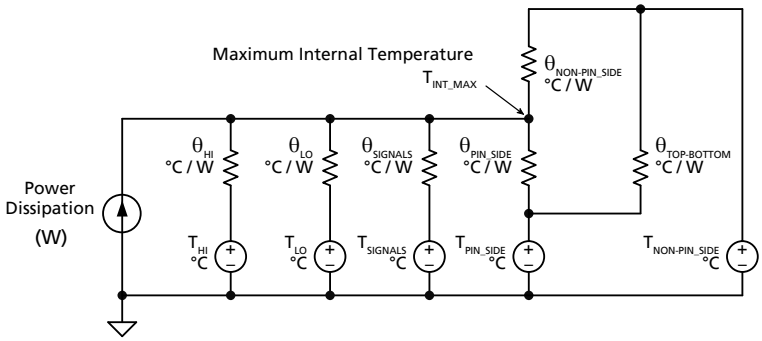


Figure 21 — *Two-sided cooling thermal model*

Symbol	Thermal Impedance (°C / W)	Definition of Estimated Thermal Resistance
$\theta_{NON-PIN\_SIDE}$	1.4	From the hottest component inside the BCM to NON-PIN_SIDE
θ_{HI}	19	From the hottest component inside the BCM to the circuit board it is mounted on at HI
θ_{LO}	23	From the hottest component inside the BCM to the circuit board it is mounted on at LO
$\theta_{SIGNALS}$	27	From the hottest component inside the BCM to the circuit board it is mounted on at SIGNALS
θ_{PIN_SIDE}	1.4	From the hottest component inside the BCM to PIN_SIDE
$\theta_{TOP-BOTTOM}$	6.1	From NON-PIN_SIDE to PIN_SIDE

Table 1 — *Thermal impedances*

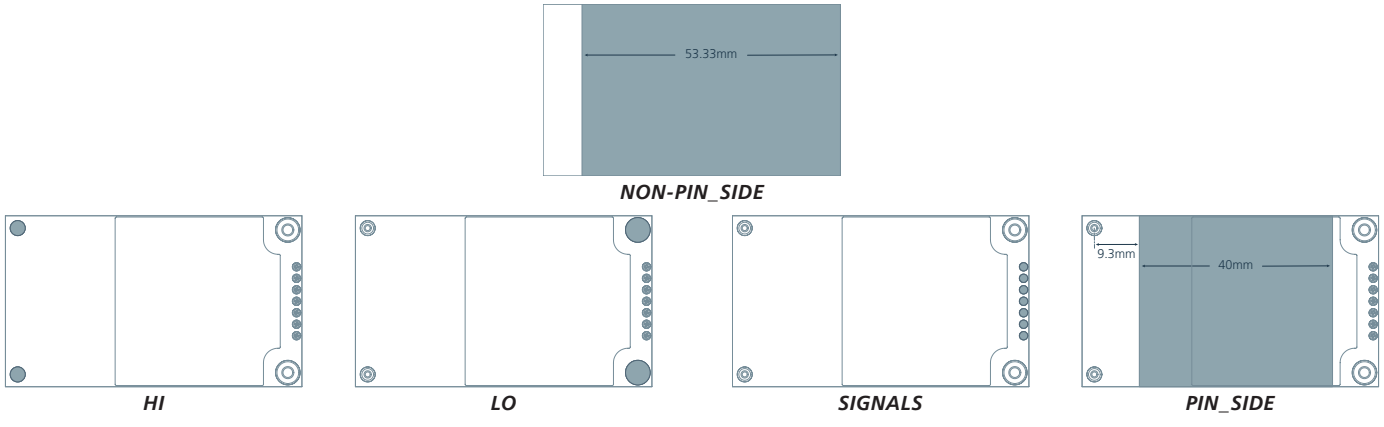


Figure 22 — *Thermal model boundary conditions; area defined as shaded*

PMBus Interface

Refer to "PMBus® Power System Management Protocol Specification Revision 1.3, Part I and II" for complete PMBus specifications details at http://pmbus.org.

Device Address

The PMBus address (ADDR terminal) should be set to one of the predetermined 16 possible addresses shown in the table below using a resistor between the ADDR terminal and SGND terminal. The BCM accepts only a fixed and persistent address and does not support SMBus address resolution protocol. At initial power up, the BCM controller will sample the address terminal voltage and will keep this address until device power is removed.

7-bit Hex Address	Resistor Value, 1% (kΩ)
50h	0.487
51h	1.05
52h	1.87
53h	2.8
54h	3.92
55h	5.23
56h	6.81
57h	8.87
58h	11.3
59h	14.7
5Ah	19.1
5Bh	25.5
5Ch	35.7
5Dh	53.6
5Eh	97.6
5Fh	316

Reported DATA Formats

The BCM controller employs a direct data format where all reported measurements are in volts, amperes, degrees Celsius or seconds. m, b and R are two's complement integers defined as follows:

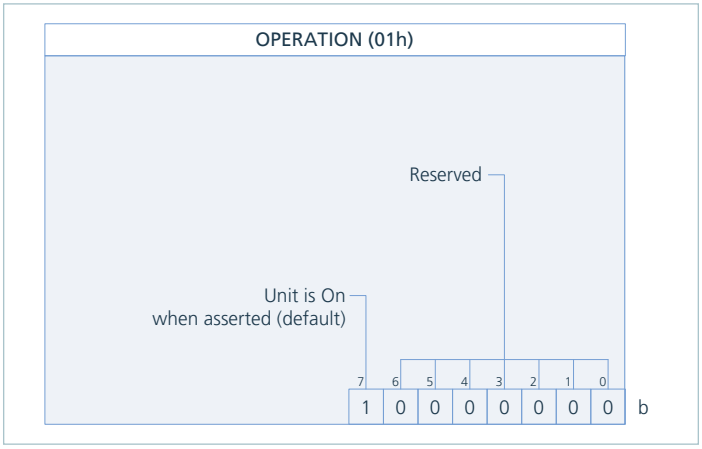
Command	Code	m	R	b
OT_FAULT_LIMIT	4Fh	1	2	0
OT_WARN_LIMIT	51h	1	2	0
TON_DELAY	60h	1	3	0
READ_VIN	88h	1	1	0
READ_VOUT	8Bh	1	2	0
READ_IOUT	8Ch	1	2	0
READ_TEMPERATURE_1	8Dh	1	0	0
READ_POUT	96h	1	0	0
READ_K_FACTOR	D1h	1	4	0

No special formatting is required when lowering the supervisory limits and warnings.

Supported Command List

Command	Code	Function	Default Data Content	SMBus Write Transaction	SMBus Read Transaction	Data Bytes	PEC Supported
OPERATION	01h	Turn BCM on or off	80h	Write Byte	Read Byte	1	Yes
ON_OFF_CONFIG	02h	Defines startup when power is applied as well as immediate on/off control over the BCM	1D	N/A	Read Byte	1	Yes
CLEAR_FAULTS	03h	Clear all faults	N/A	Send Byte	N/A	None	No
CAPABILITY	19h	PMBus® key capabilities set by factory	A0h	N/A	Read Byte	1	Yes
QUERY	1Ah	Returns Query data as specified in PMBus Specification 1.3	N/A	N/A	Block Write/Block Read Process Call	1	Yes
COEFFICIENTS	30h	Read m, b and R coefficients for parametric commands	N/A	N/A	Block Write/Block Read Process Call	5	Yes
STATUS_BYTE	78h	Summary of faults	00h	Write Byte	Read Byte	1	Yes
STATUS_WORD	79h	Summary of fault conditions	00h	Write Word	Read Word	2	Yes
STATUS_VOUT	7Ah	Low side voltage fault status	00h	N/A	Read Byte	1	Yes
STATUS_IOUT	7Bh	Overcurrent fault status	00h	N/A	Read Byte	1	Yes
STATUS_INPUT	7Ch	Overvoltage and undervoltage fault status	00h	N/A	Read Byte	1	Yes
STATUS_TEMPERATURE	7Dh	Overtemperature and undertemperature fault status	00h	N/A	Read Byte	1	Yes
STATUS_CML	7Eh	PMBus communication fault	00h	Write Byte	Read Byte	1	Yes
STATUS_MFR_SPECIFIC	80h	Other BCM status indicator	00h	Write Byte	Read Byte	1	Yes
READ_VIN	88h	Reads high side voltage	FFFFh	N/A	Read Word	2	Yes
READ_VOUT	8Bh	Reads low side voltage	FFFFh	N/A	Read Word	2	Yes
READ_IOUT	8Ch	Reads low side current	FFFFh	N/A	Read Word	2	Yes
READ_TEMPERATURE_1	8Dh	Reads internal temperature	FFFFh	N/A	Read Word	2	Yes
READ_POUT	96h	Reads low side power	FFFFh	N/A	Read Word	2	Yes
MFR_ID	99h	Internal controller ID	"VI"	N/A	Block Read	2	Yes
MFR_MODEL	9Ah	Internal controller or BCM model	Part Number	N/A	Block Read	18	Yes
MFR_DATE	9Dh	Internal controller or BCM manufacturing date	"YYWW"	N/A	Block Read	4	Yes
MFR_SERIAL	9Eh	Internal controller or BCM serial number	Serial Number	N/A	Block Read	16	Yes

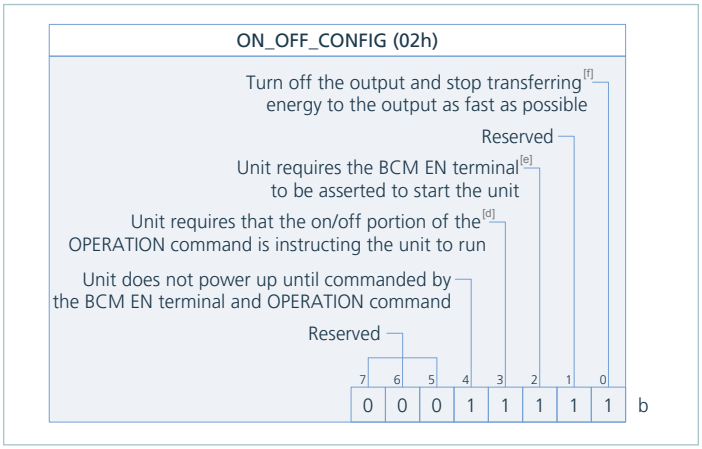
OPERATION Command (01h)



The OPERATION command and the BCM EN terminal can both be used to turn on and off the connected BCM. Note that the Host OPERATION command will not enable the BCM if the BCM EN terminal is disabled in hardware with respect to the pre-set terminal polarity. The OPERATION command provides ON/OFF control only with the BCM EN terminal active.

If synchronous start up is required in the system, it is recommended to use the command from Host PMBus or the BCM EN terminal in order to achieve simultaneous array start up.

ON_OFF_CONFIG Command (02h)

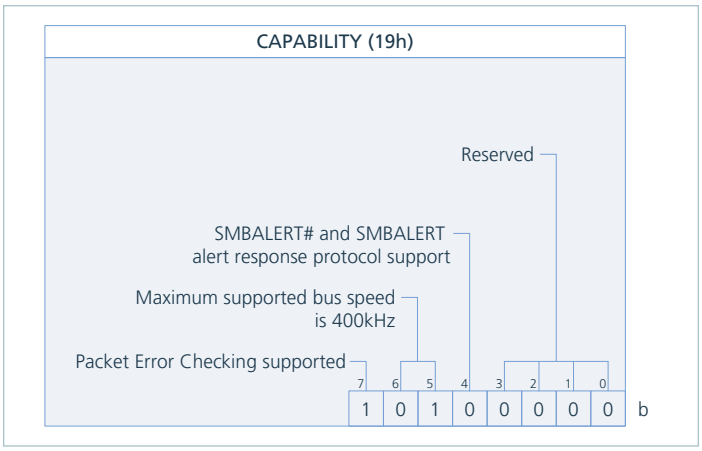


[d] The BCM EN terminal is ALWAYS to be asserted for power up.
[e] With respect to the BCM EN terminal if used in system.
[f] The BCM powertrain once disabled cannot sink current.

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re-asserted again once cleared. All faults are latched once asserted in the BCM. Registered faults will not be cleared when disabling the BCM powertrain by the EN terminal, sending the OPERATION command, or by lowering the high-side voltage below the undervoltage lockout threshold. There is no data byte for this command.

CAPABILITY Command (19h)



The BCM returns a default value of A0h. This value indicates that the PMBus® frequency supported is up to 400kHz and that Packet Error Checking (PEC) is supported. SMBALERT# is not supported.

QUERY Command (1Ah)

The QUERY command is used to ask a PMBus device if it supports a given command, and if so, what data formats it supports for that command. This command uses the Block Write – Block Read format described in the PMBus Specification 1.3 Part II.

Bit	Value	Description
7	0	Command not supported
	1	Command supported
6	0	Command not supported for write
	1	Command supported for write
5	0	Command not supported for read
	1	Command supported for read
4:2	000	LINEAR11, ULINEAR16, or SLINEAR16 [g]
	001	16 bit signed number
	010	IEEE Half Precision Floating Point format
	011	Direct Mode format
	100	8 bit unsigned integer
	101	VID Mode format
	110	Manufacturer specific format
	111	Command does not return numeric data [h]
1:0	XX	Reserved

[g] As defined by specification of the command being queried.
[j] Also used for commands that return blocks of data or the SEND BYTE protocol

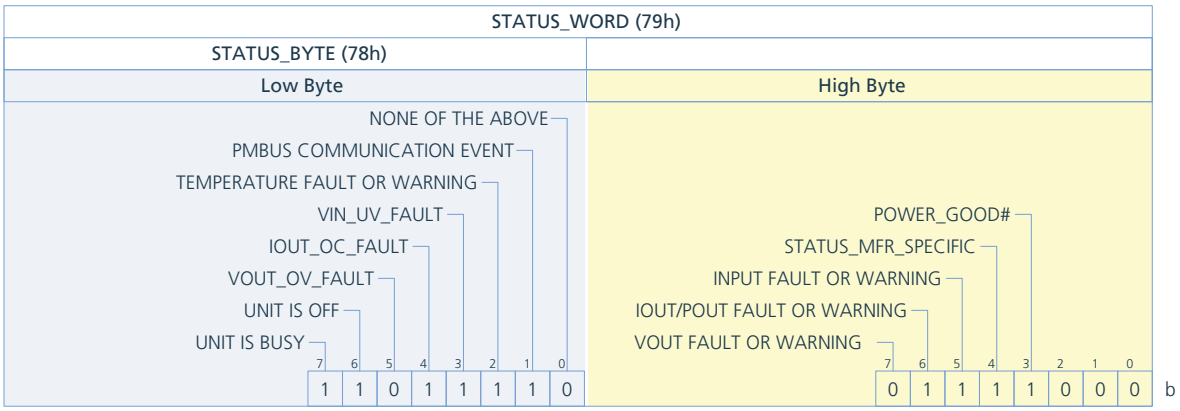
COEFFICIENTS Command (30h)

The command returns the coefficients (m, R and B) for data in the DIRECT Mode format. The command is read-only and uses the Block Write/Block Read process call. The write portion of the process call is composed of two bytes, including the command code of interest followed by a byte indicating the data access type of the requested coefficients. The command returns 5 bytes corresponding to the m, R and B coefficients during the read portion of the process call. The coefficient values are also given in the Reported Data Formats section of this document.

Write portion (byte count is always 2)		
Byte	**Value**	**Description**
1	User input	Command code of interest
2	00	Retrieve coefficients for write transaction
	01	Retrieve coefficients for read transaction
Read portion (byte count is always 5)		
Byte	**Value**	**Description**
1	Varies per command	Lower byte of m coefficient
2	Varies per command	Upper byte of m coefficient
3	Varies per command	Lower byte of B coefficient
4	Varies per command	Upper byte of B coefficient
5	Varies per command	R coefficient

It is recommended that the QUERY command be executed prior to the COEFFICIENTS command to confirm support for the command of interest and to determine the applicable data access types. Unsupported commands, unsupported command transaction types or commands not following the DIRECT Mode format will return 0 for all m, R and B coefficients and will set the STATUS_CML Invalid/Unsupported Data Received bit.

STATUS_BYTE (78h) and STATUS_WORD (79h)



All fault or warning flags, if set, will remain asserted until cleared by the Host or once the BCM input power is removed.

This includes undervoltage fault, overvoltage fault, overtemperature fault, overtemperature warning, undertemperature fault and communication faults.

Asserted status bits in all status registers, with the exception of STATUS_VOUT, STATUS_INPUT, STATUS_TEMPERATURE and STATUS_IOUT, can be individually cleared. This is done by sending a data byte with one in the bit position corresponding to the intended warning or fault to be cleared. Status bits in the STATUS_WORD and STATUS_BYTE cannot be individually cleared, with the exception of the UNIT IS BUSY bit by writing 80h to STATUS_BYTE (78h). Refer to the PMBus® Power System Management Protocol Specification - Part II - Revision 1.3 for details.

The POWER_GOOD# bit reflects the state of the device and does not reflect the state of the POWER_GOOD# signal limits. The POWER_GOOD_ON COMMAND (5Eh) and POWER_GOOD_OFF COMMAND (5Fh) are not supported. The POWER_GOOD# bit is set, when the BCM is not in the active state, to indicate that the powertrain is inactive and not switching. The POWER_GOOD# bit is cleared, when the BCM is in the active state, 5ms after the powertrain is activated allowing for soft start to elapse.

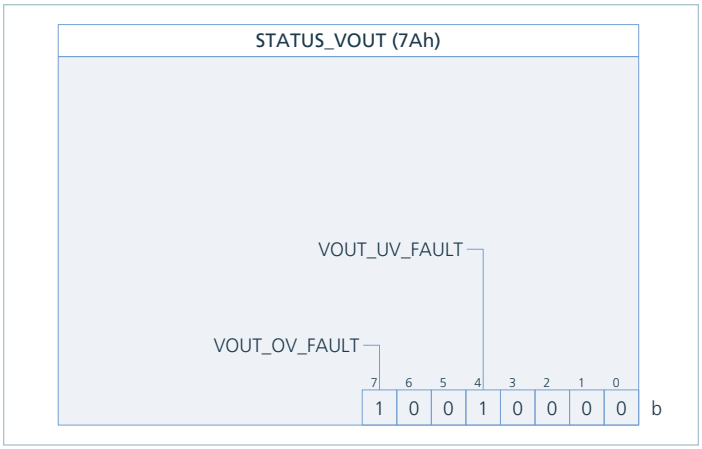
POWER_GOOD# and UNIT IS OFF bits cannot be cleared as they always reflect the current state of the device.

Fault reporting, such as SMBALERT# signal output, and Host notification by temporarily acquiring bus parent status is not supported.

If the BCM is powered by $V_{HI} \geq V_{HI\_CONTROL}$, it will retain the last telemetry data and this information will be available to the user via a PMBus Status request. This is in agreement with the PMBus standard, which requires that status bits remain set until specifically cleared. Note that in the case where the BCM V_{IN} is lost, i.e., $V_{HI\_CONTROL} \leq V_{HI} \leq V_{HI\_UVLO+}$, the status will always indicate an undervoltage fault, in addition to any other fault that occurred.

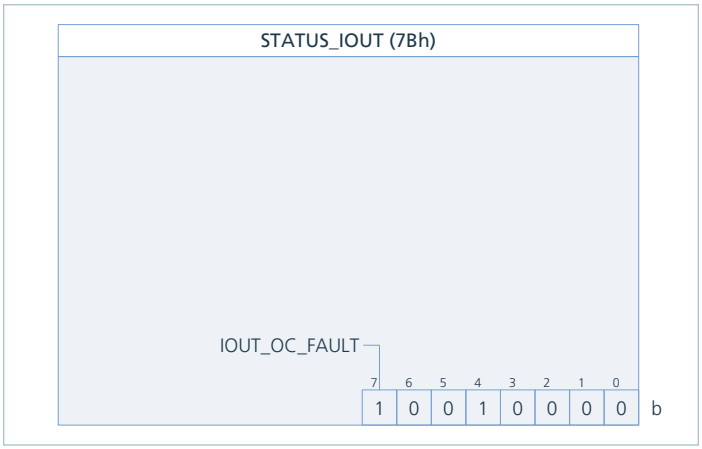
NONE OF THE ABOVE bit will be asserted if either the STATUS_MFR_SPECIFIC (80h) or the High Byte of the STATUS WORD is set.

STATUS_VOUT (7Ah)



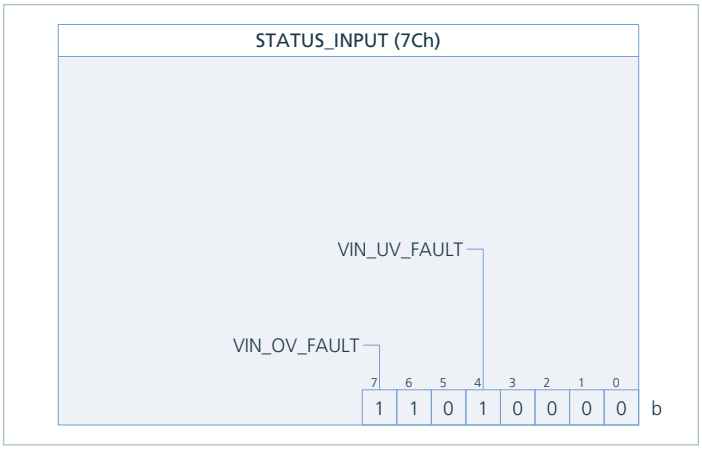
Unspecified bits are not supported. A one indicates a fault.

STATUS_IOUT (7Bh)



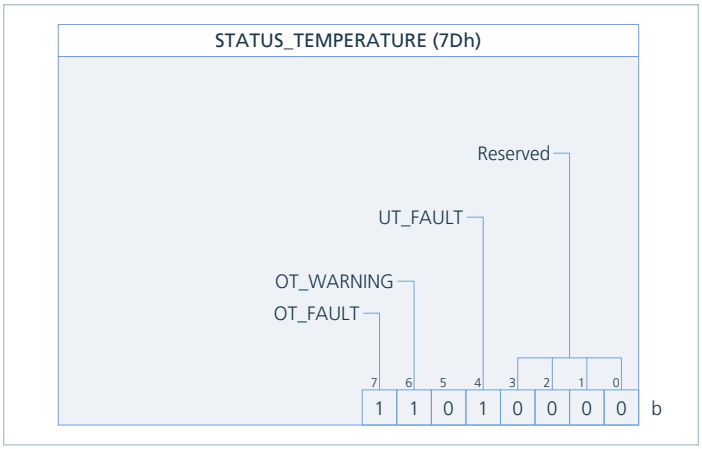
Unspecified bits are not supported. A one indicates a fault.

STATUS_INPUT (7Ch)



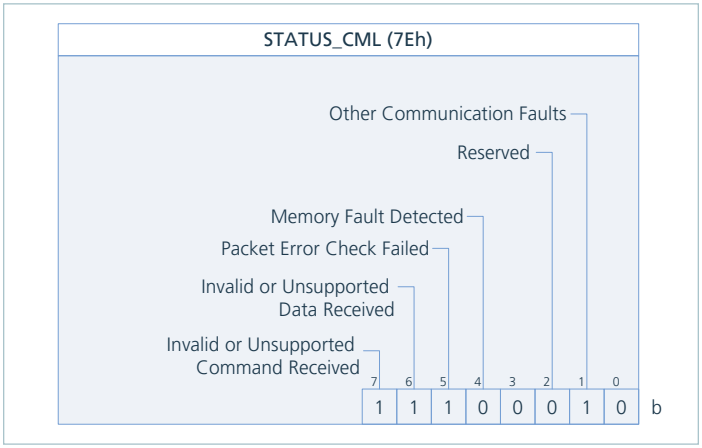
Unspecified bits are not supported. A one indicates a fault.

STATUS_TEMPERATURE (7Dh)



Unspecified bits are not supported. A one indicates a fault.

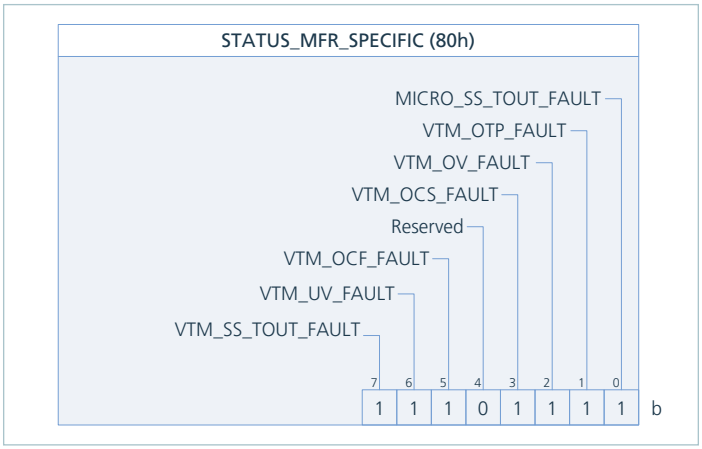
STATUS_CML (7Eh)



Unspecified bits are not supported. A one indicates a fault.

The STATUS_CML data byte will be asserted when an unsupported PMBus® command or data or other communication fault occurs.

STATUS_MFR_SPECIFIC (80h)



The BCM consists of a supervisory microcontroller and a powertrain controller. This register reports powertrain controller faults. The VTM_SS_TOUT_FAULT, if asserted, indicates a soft-start timeout fault. VTM_UV_FAULT and VTM_OV_FAULT report undervoltage and overvoltage fault conditions reported by the powertrain controller. In the event of an short circuit condition, the VTM_OCF_FAULT will be asserted. An overcurrent condition is indicated by the VTM_OCS_FAULT bit. The powertrain controller monitors the BCM internal temperature. An overtemperature shut-down condition is indicated by assertion of the VTM_OTP_FAULT bit.

The MICRO_SS_TOUT_FAULT bit, if asserted, refers to a soft-start time-out condition detected by the supervisory controller.

Unspecified bits are not supported. A one indicates a fault.

READ_VIN Command (88h)

The READ_VIN command returns the BCM's high-side voltage V_{HI} in direct format.

READ_VOUT Command (8Bh)

The READ_VOUT command returns the BCM's low-side voltage V_{LO} in direct format.

READ_IOUT Command (8Ch)

The READ_IOUT command returns the BCM's low-side current I_{LO} in direct format.

READ_TEMPERATURE_1 Command (8Dh)

The READ_TEMPERATURE_1 command returns the BCM's temperature in direct format.

READ_POUT Command (96h)

The READ_POUT command returns the BCM's low-side power P_{LO} in direct format.

PMBus Communication Fault

Module Behavior

Corrupted data, unrecognized commands or other PMBus® protocol violations have no impact on powertrain functionality.

PMBus Reporting Characteristics

The below tables summarize data transmission and data content faults as implemented in the BCM.

Section	Description	Response to Host		STATUS_BYTE	STATUS_CML			Notes
		NACK	FFh	CML	Other Fault	Unsupported Data	PEC Failed	
10.8.1	Corrupted data						X	
10.8.2	Sending too few bits			X	X			
10.8.3	Reading too few bits			X	X			
10.8.4	Host sends or reads too few bytes			X	X			
10.8.5	Host sends too many bytes	X		X				
10.8.6	Reading too many bytes		X	X	X			
10.8.7	Device busy	X	X					Device will ACK own address; BUSY bit in STATUS_BYTE even if STATUS_WORD is set

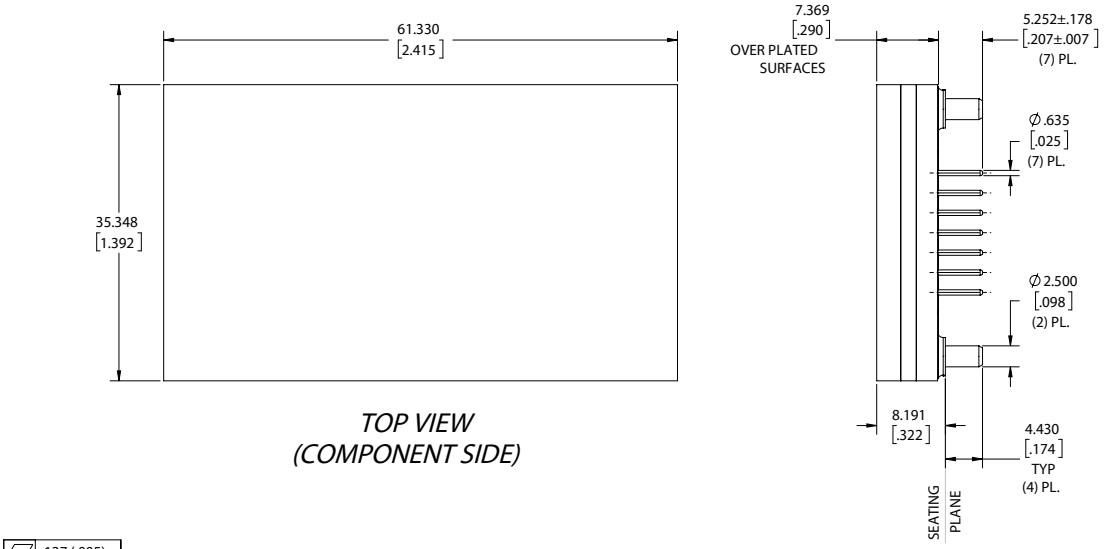
Table 2 — *Data transmission faults*

Section	Description	Response to Host	STATUS_BYTE	STATUS_CML			Notes
		NACK	CML	Other Fault	Unsupported Command	Unsupported Data	
10.9.1	Improperly set read bit in the address byte	X	X	X			No Response
10.9.2	Unsupported command code	X	X		X		
10.9.3	Invalid or unsupported data		X			X	
10.9.4	Data out of range		X			X	
10.9.5	Reserved bits						No response; not a fault

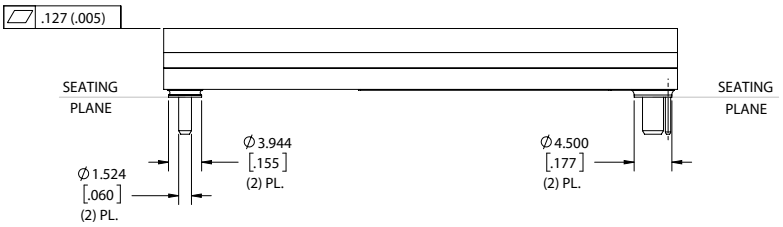
Table 3 — *Data content faults*

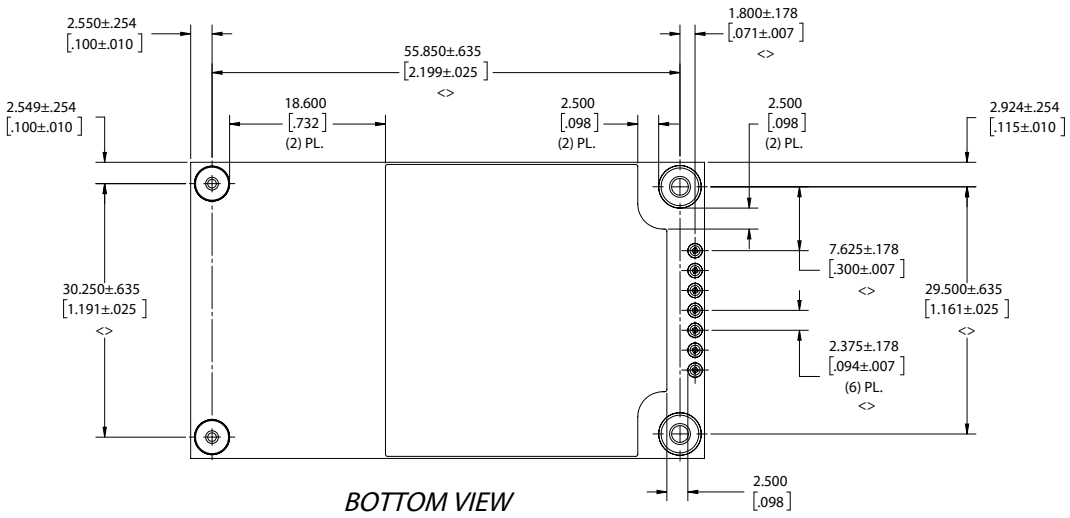
Outline Drawing

BCM6135 TC9
(Reference DWG # 49103 Rev 2)



TOP VIEW
(COMPONENT SIDE)



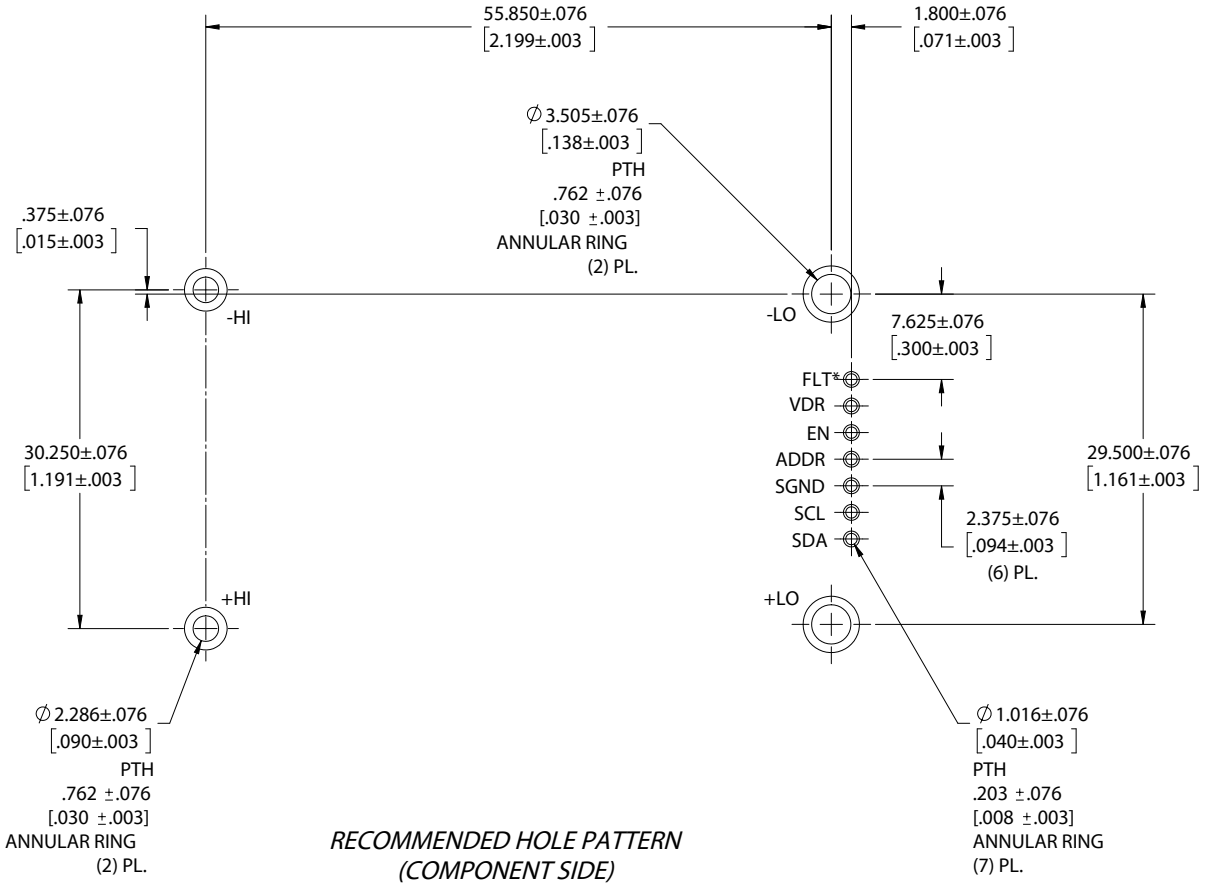


BOTTOM VIEW

NOTES:
1- MIN THERMAL-INTERFACE COMPLIANCE: .254/[.010"]
2- <> DENOTES CRITICAL CHARACTERISTIC
3- UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM [INCH]
4- TOLERANCES ARE:
DECIMALS
X.XX [X.XX] = ±0.25 [0.01]
X.XXX [X.XXX] = ±0.127 [0.005]
ANGLES = ±1°

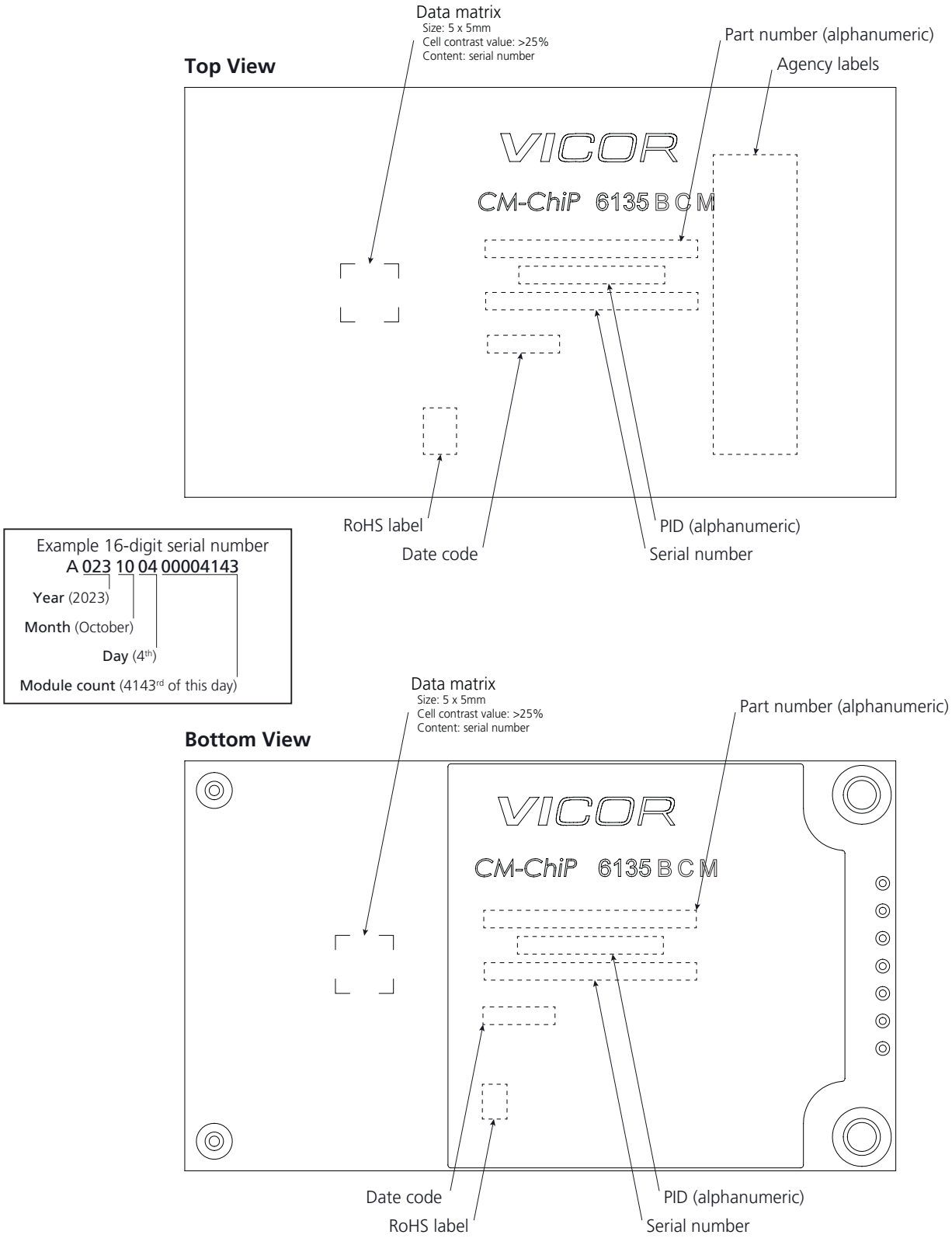
Recommended Hole Pattern

BCM6135 TC9
(Reference DWG # 49103 Rev 2)



RECOMMENDED HOLE PATTERN
(COMPONENT SIDE)

Package Marking Specification



Revision History

Revision	Date	Description	Page Number(s)
1.0	06/14/24	Initial release	n/a
1.1	09/05/24	Corrected output ripple and output resistance specifications Revised list of supported commands	5, 6 23, 25
1.2	10/07/24	Updated features and benefits	1

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