DCM™ DC-DC Converter

DCM3735S58E16L0AN2

48V to Point-of-Load Automotive Regulated DC Converter

Features & Benefits

- Wide input range 35 – 58V_{DC}
- Wide output range 8 – 16V_{DC}
- 297.4kW/L typical power density
- 96.5% peak efficiency
- Up to 2kW continuous operation
- PMBus® compatible telemetry
- Internal voltage, current and temperature shut down
- ZVS Buck-Boost: regulation
- Sine Amplitude Converter: current multiplication
- Constant current operation for battery charging
- Automotive APQP process + product development integration
- Integrated AECQ-100 qualified Vicor controller

Typical Applications

- Electric and Mild-Hybrid Vehicles
- Decentralized Architectures

Product Ratings	
V_{IN} = 35 – 58V	P_{OUT} = 2000W
V_{OUT} = 14V Nominal (8.0 – 16.0V)	I_{OUT} = 160A (max)

Product Description

The DCM is a regulated, non-isolated DC-DC converter module operating from a semi-regulated 35 – 58V input to generate a regulated point-of-load (PoL) output range of 8.0 – 16.0V. The DCM in the SM-ChiP package configuration utilizes the Vicor patented zero-voltage switching (ZVS) Buck-Boost regulator stage followed by the Sine Amplitude Converter (SAC™).

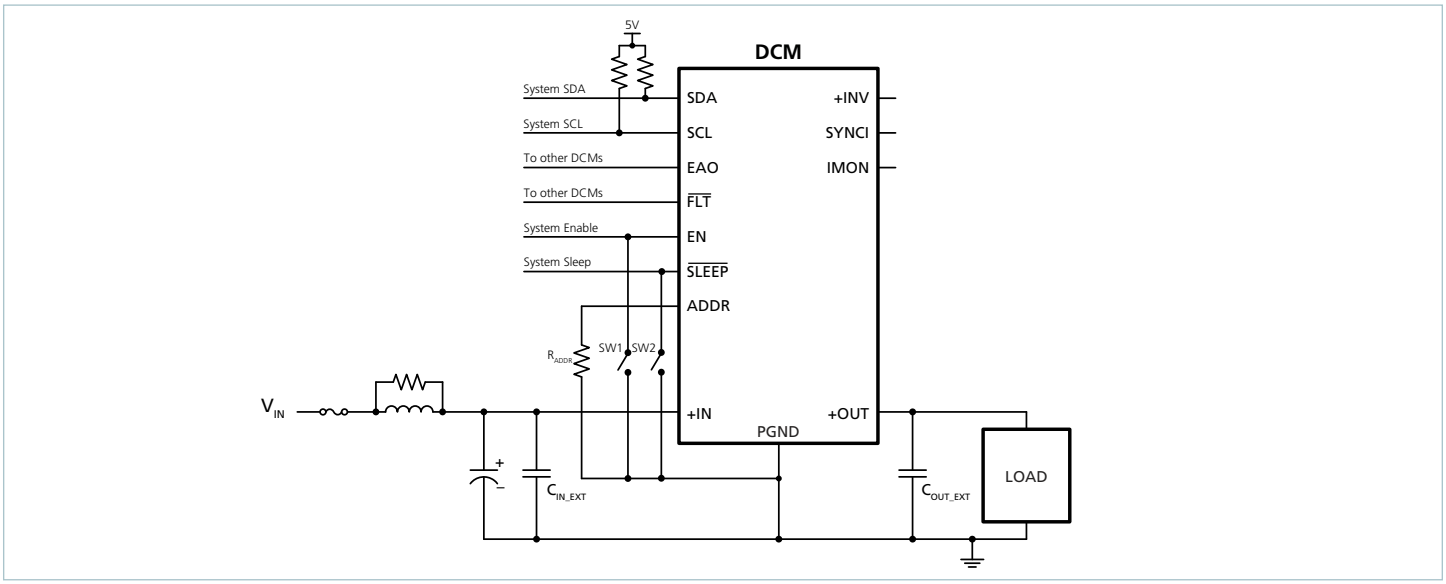
Leveraging the thermal density benefits of the Vicor SM-ChiP packaging technology, the DCM offers flexible thermal management options with very low top- and bottom-side thermal impedances. Thermally adept SM-ChiP based power components enable customers to achieve low-cost power system solutions with previously unattainable system size, weight and efficiency attributes quickly and predictably.

Package Information

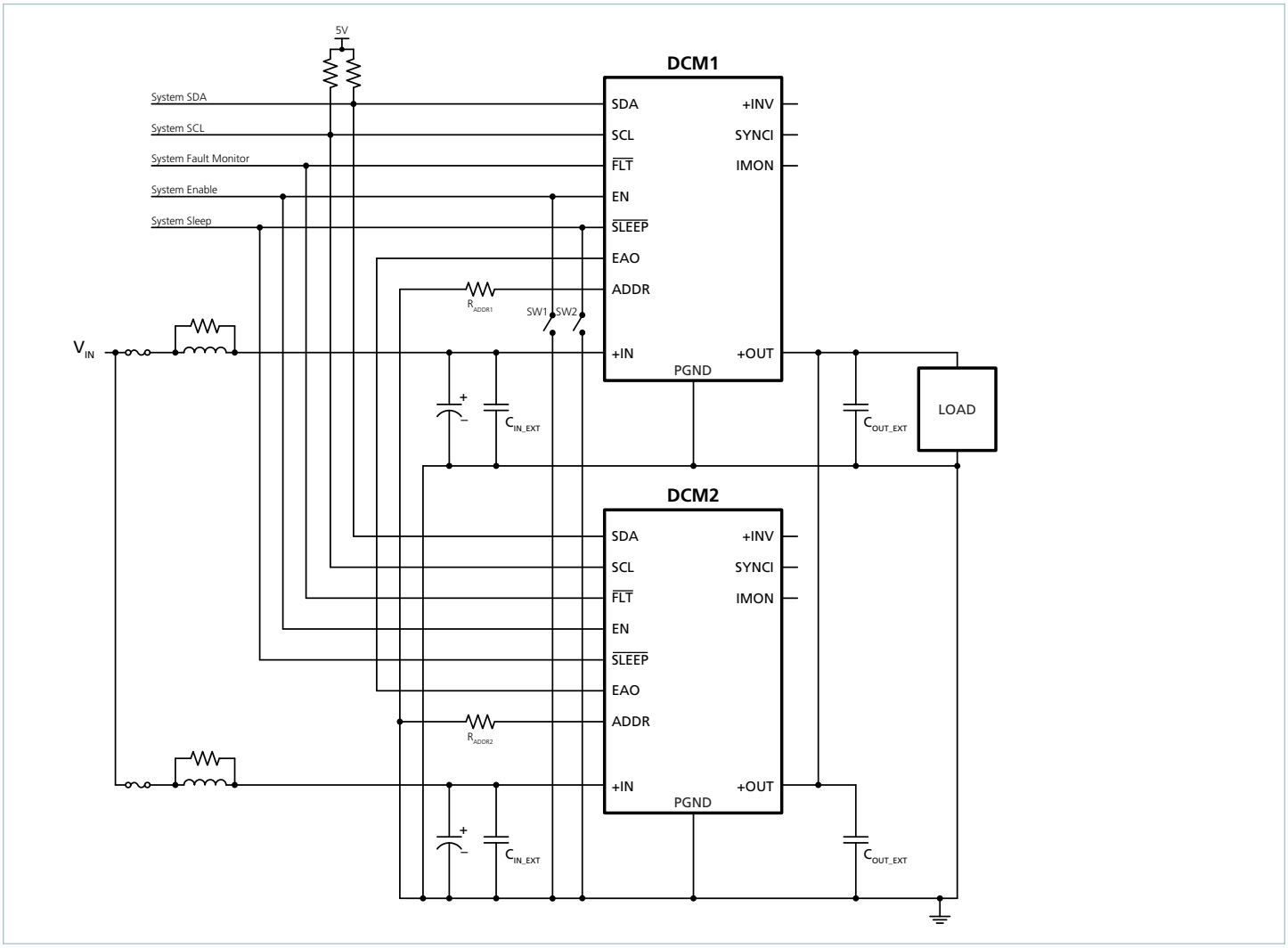
- 36.7 x 35.4 x 5.2mm SM-ChiP™
- Weight: 29g

Note: Product images may not highlight current product markings and cosmetic features.

Typical Application



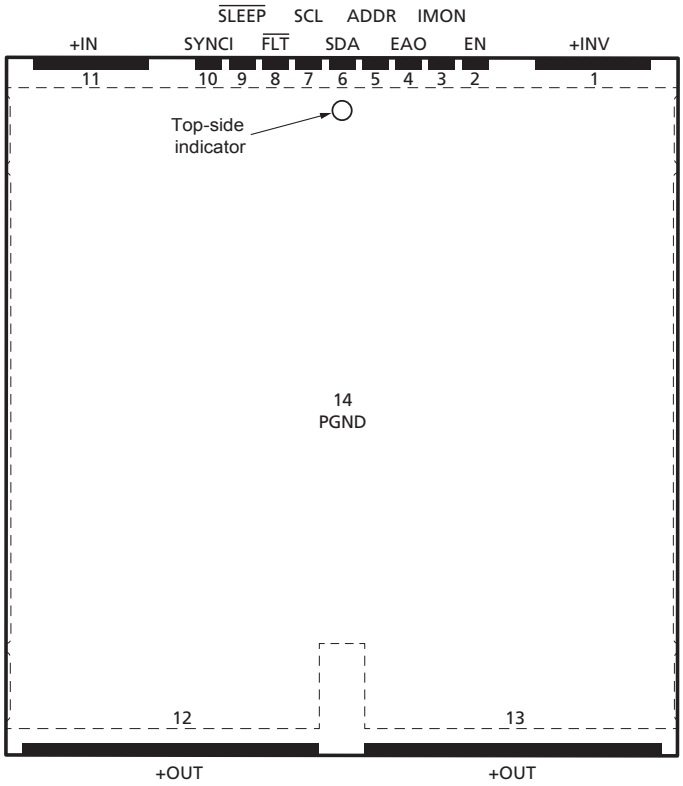
DCM3735 to point-of-load



DCM3735s in a high-power array

Terminal Configuration

Top View



DCM3735 SM-ChiP™

Terminal Descriptions

Signal Name	Terminal Number	Terminal Functions
+INV	1	Intermediate power terminal
EN	2	DCM enable control
IMON	3	Factory use only; leave floating
EAO	4	Transconductance error amplifier output and powertrain modulator control node
ADDR	5	I^2C address assignment
SDA	6	Digital serial communication data terminal
SCL	7	Digital serial communication clock terminal
$\overline{FLT}$ [a]	8	Fault Flag; pulled low when a fault is detected
$\overline{SLEEP}$	9	Sleep mode control terminal; when held low, the unit will exhibit low quiescent current consumption at the +OUT power terminals
SYNCI	10	Factory use only; leave floating
+IN	11	Positive input power terminal
+OUT	12, 13	Positive output power terminal
PGND	14 [b]	Power ground

[a] Overbar ($\overline{FLT}$) or star (FLT*) marking signify an active low designation.
[b] Terminal 14 represents the package top and bottom conductive plating. Refer to product outline for additional details.

Part Ordering Information

Part Number	Temperature Grade	Tray Size
DCM3735S58E16L0**A**N2	**A** = –40 to 125°C	323 x 136 x 12mm 12 parts per tray Vicor PN 49556

Storage and Handling Information

Note: For compressive loading refer to Application Note AN:036, "Recommendations for Maximum Compressive Force of Heat Sinks."
For handling and assembly processing, and for rework considerations refer to Application Note AN:701, "SM-ChiP Reflow Soldering Recommendations."

Attribute	Comments	Specification
Storage Temperature Range		–40 to 125°C
Operating Internal Temperature Range (T_{INT})		–40 to 125°C
Weight		29g
MSL Rating		MSL 4, 245°C maximum reflow temperature
ESD Rating	Human Body Model JEDEC JS-001-2023	Class 2 ≥2kV
	Charged Device Model JEDEC JS-002-2022	Class 2a ≥500V

Agency Approvals

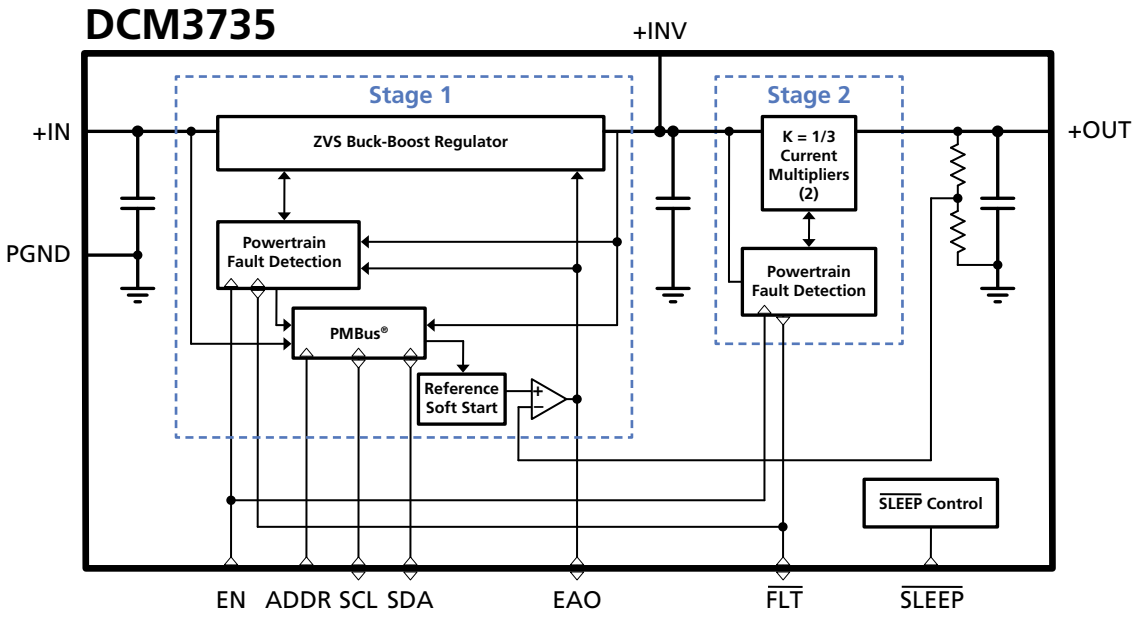
Attribute	Comments	Value	Unit
MTTF	MIL-HDBK-217F Parts Count, Ground Benign	2.43	MHrs
	Telcordia SR-332 Issue 2, Method I Case 3, Ground Benign	5.69	
FIT	MIL-HDBK-217F Parts Count, Ground Benign	412	FIT
	Telcordia SR-332 Issue 2, Method I Case 3, Ground Benign	176	
Agency Approvals/Standards			
	UKCA, electrical equipment (safety) regulations		
	CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable		

Absolute Maximum Ratings

The ABSOLUTE MAXIMUM ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Operating beyond rated operating conditions for an extended period of time may affect device reliability. Positive terminal currents represent current flowing out of the terminal.

Parameter	Comments	Min	Max	Unit
+INV	Non-operating	–0.3	60	V
EN		–0.3	5.5	V
EAO		–0.3	5.5	V
SCL, SDA, ADDR		–0.3	5.5	V
$\overline{FLT}$		–0.3	5.5	V
		–20	20	mA
$\overline{SLEEP}$		–0.3	6.2	V
+IN	Non-operating	–0.3	70	V
+OUT	Continuous, non-operating	–0.3	23.3	V

Functional Block Diagram



Electrical Specifications

Specifications apply over all line, trim, and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C (A-Grade). All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Input Power Specifications						
Input Voltage Range	V_{IN}	Typical value defines product V_{IN-NOM}	**35**	48	**58**	V
Input Voltage Slew Rate	dV_{IN}/dt				**1**	V/µs
Input Voltage for ADDR Latch	V_{IN_ADDR}	Initial power up			**12**	V
No-Load Power Dissipation	P_{NL}	EN high, V_{IN} = 48.0V, V_{OUT} = 14V		12.6	18.09	W
Quiescent Current, Input	I_{QC_IN}	EN low, V_{IN} = 48.0V		11		mA
Quiescent Current, Output	I_{QC_OUT}	EN low, V_{IN} < V_{OUT}; $\overline{SLEEP}$ low			25	µA
Input Current	I_{IN_DC}	I_{OUT} = 143A, V_{IN} = 48.0V, V_{OUT} = 14V		43.5	44.13	A
Input Capacitance (Internal)	C_{IN_INT}	Effective value, V_{IN} = 48.0V		8.86		µF
Input Capacitance (Internal) ESR	R_{C_IN}	Effective value, V_{IN} = 48.0V, 1MHz		0.2		mΩ
Output Power Specifications						
Output Current Set Point	I_{OUT_SET}	Constant current limit, V_{OUT} = 14V, P_{OUT} = 2000W		142		A
Output Voltage Trim Range	V_{OUT}	No load; typical value defines product $V_{OUT-NOM}$	**8**	14	**16**	V
Output Voltage Load Regulation	$V_{OUT-REG-LOAD}$	For load > 10%		0.15	**0.25**	%
Output Voltage Line Regulation	$V_{OUT-REG-LINE}$			0.01	**0.02**	%
Rated Output Current, Continuous	I_{OUT}	V_{OUT} ≤ 12.5V			**160**	A
Rated Output Power, Continuous	P_{OUT}	12.5V < V_{OUT} < 14V			**2000**	W
Array Size	n_{ARRAY}				**4**	DCMs
Switching Frequency, Buck-Boost Stage 1	F_{SW1}	V_{IN} = 48V, V_{OUT} = 14V, I_{OUT} = 143A	**0.783**	0.870	**0.95**	MHz
		Over rated line, continuous load, trim and temperature, exclusive of burst mode	**0.3**		**1.4**	MHz
Switching Frequency, Current Multiplier Stage 2	F_{SW2}	V_{IN} = 48V, V_{OUT} = 14V, I_{OUT} = 143A	**1.9**	2.11	**2.3**	MHz
		Over rated line, continuous load, trim and temperature	**1.9**		**2.5**	MHz
Transfer Ratio, Current Multiplier Stage 2	K			1/3		V/V
Minimum Off Time to Restart	t_{OFF}	If externally disabled with EN or $\overline{FLT}$	**0**		**500**	µs
Output Voltage Rise Time	t_{SS}	From soft start begin to V_{OUT} settled to within 5%	**11**	16	**26**	ms
Output Turn-On Delay	t_{ON}	From EN release to soft-start ramp, V_{IN} pre-applied		1.5		ms
Efficiency, Ambient	η_{AMB}	V_{IN} = 48V, V_{OUT} = 14V, I_{OUT} = 143A, T_{CASE} = 25°C	95.3	95.7		%
		V_{IN} = 48V, V_{OUT} = 14V, I_{OUT} = 71.5A, T_{CASE} = 25°C	96.0	96.5		
Efficiency, Hot	η_{HOT}	V_{IN} = 48V, V_{OUT} = 14V, I_{OUT} = 71.5A, T_{CASE} = 100°C	95.6	96		%
Output Capacitance (Internal)	C_{OUT_INT}	Effective value, V_{OUT} = 14.0V		55		µF
Output Capacitance (Internal) ESR	R_{COUT}	Effective value, V_{OUT} = 14.0V		0.121		mΩ
Load Capacitance (Electrolytic)	C_{LOAD_ALEL}				**10**	mF
Load Capacitance (Ceramic)	C_{LOAD_CER}	Nominal value; ESR ≤ 100mΩ			**200**	µF
Load Capacitance (Total)	C_{LOAD_TOTAL}				**10.2**	mF

Electrical Specifications (Cont.)

Specifications apply over all line, trim, and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C (A-Grade). All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Fault Detection and Response						
Input Undervoltage Threshold Rising	V_{IN_UVLO+}	Powertrain recovery	**28.2**	29.5	**31**	V
Input Undervoltage Hysteresis	$V_{IN\_UVLO\_HYS}$	Powertrain shut down	**0.7**	0.9	**1.1**	V
Input Overvoltage Threshold Rising	V_{IN_OVLO+}	Powertrain shut down	**61.2**	64.5	**67.5**	V
Input Overvoltage Hysteresis	$V_{IN\_OVLO\_HYS}$	Powertrain recovery	**1.83**	2	**2.3**	V
Minimum Current-Limited V_{OUT}	V_{OUT_UVP}				**5**	V
Overtemperature Shut Down	T_{OT}		125			°C
Overtemperature Restart Hysteresis	T_{OT_HYS}			30		°C
EAO Overload Threshold	V_{EAO_OL}		**3.23**	3.3		V
EAO Overload Timeout	t_{EAO_OL}	EAO continuously above V_{EAO_OL}		1		ms
Output Voltage Negative Fault Threshold	V_{OUT_NEG}	Level threshold to trigger fault	–0.45	–0.25	–0.15	V
Output Voltage Threshold to Re-Enable V_{OUT_NEG} Fault	$V_{OUT\_NEG\_RE\text{-}ARM}$	Positive-going V_{OUT} which re-arms the V_{OUT_NEG} fault	**1**	2.25	**3**	V
Overcurrent Shut Down	I_{OC}	I_{OC1} when detected by ZVS buck-boost stage; I_{OC2} when detected by current multiplier stage	164	190		A
Overcurrent Timeout	t_{IOC}	Output current above I_{OC}	**1**	4		ms
Output OVP Turn-OFF	V_{OUT_OVP}	Relative to module +INV terminal	**52.25**		**54.58**	V
Output OVP Relative	$\%_{EAIN\_HI}$	Relative to the VOUT_COMMAND; inactive during start up and for t_{EAIN_HI} after a VOUT_COMMAND	**4**	15		%
Output OVP Relative Timeout	t_{EAIN_HI}	Blanking time for output OVP relative shut down following VOUT_COMMAND		**2.1**		s
Fault Response Time	t_{FAULT}	Excluding t_{EAO_OL} and t_{IOC} timeout periods		**1**		µs
Stage 1 Fault Recovery Time	$t_{FAULT1\_RECOVERY}$	Excluding I_{OC2} and overtemperature shut downs		**30**		ms
Stage 2 Fault Recovery Time	$t_{FAULT2\_RECOVERY}$	Recovery from stage-2 current multiplier OVP, I_{OC2} and I_{SHORT} shut downs only		**135**		ms

Electrical Specifications (Cont.)

Specifications apply over all line, trim, and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C (A-Grade). All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
PMBus® Characteristics						
READ_VIN Accuracy		Across all line, trim and load	**–5**		**5**	%
READ_VIN Resolution				125		mV
READ_VIN Functional Range			**0**		**75**	V
READ_VOUT Accuracy		Across all line, trim and load	**–5**		**5**	%
READ_VOUT Resolution				31.25		mV
READ_VOUT Functional Range			**0**		**88**	V
READ_IOUT Accuracy		Across all line and trim, >50% load	**–15**		**15**	%
READ_IOUT Resolution				250		mA
READ_IOUT Functional Range			**0.5**		**160**	A
READ_TEMPERATURE Accuracy		Disabled, with T_{CASE} = 25°C	**–6**		**6**	°C
READ_TEMPERATURE Functional Range			**–273**		**184**	°C
VOUT_COMMAND Accuracy		Across all line and trim at no load	**–5**		**5**	%
VOUT_COMMAND Resolution				1.95		mV
VOUT_COMMAND Functional Range			**8**		**16**	V
IOUT_OC_FAULT_LIMIT Accuracy		Across all line and trim, >50% load	**–15**		**15**	%
IOUT_OC_FAULT_LIMIT Resolution				0.5		A
IOUT_OC_FAULT_LIMIT Functional Range			**0**		**255.5**	A
VOUT_TRANSITION_RATE Accuracy		Across all line and trim at no load	**–5**		**5**	%
VOUT_TRANSITION_RATE Resolution				0.25		mV/us
VOUT_TRANSITION_RATE Functional Range			**1**		**50**	mV/us
STORE_USER_CODE Capacity		Storage of user defined commands			**8**	Writes

Electrical Specifications (Cont.)

Specifications apply over all line, trim, and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C (A-Grade). All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Enable: EN						
EN Input High Voltage	V_{EN_HIGH}		**1.1**			V
EN Input Low Voltage	V_{EN_LOW}				**0.7**	V
EN Source Current	I_{EN}	Pull up to ~5V			200	µA
Control Node: EAO						
EAO Voltage Range	V_{EAO}		**0**		**3.15**	V
EAO Current Drive	I_{EAO}		**0.3**		**0.6**	mA
EAO Pulse Skip Threshold	V_{EAO_SKIP}	Lower side of hysteretic range		0.4		V
EAO Sink Current	I_{EAO_FAULT}	Pull down to 0V while shut down due to a fault		450		µA
Serial Clock: SCL **Serial Data: SDA**						
Serial Input Range	V_{SERIAL}		**3.3**		**5**	V
SCL Frequency	f_{SCL}		**10**		**400**	kHz
Input High Voltage	V_{IH}		**1.35**			V
Input Low Voltage	V_{IL}				**0.8**	V
Output Low Voltage	V_{OL}	Sinking 4mA			**0.4**	V
Address: ADDR						
Address Registration Delay	t_{SADDR_DLY}	From V_{IN} crossing V_{IN_ADDR}		10.5	**30**	ms
Fault: $\overline{FLT}$						
Fault Input High Voltage	$V_{\overline{FLT}\_IN\_HIGH}$		**1.15**			V
Fault Input Low Voltage	$V_{\overline{FLT}\_IN\_LOW}$	To externally induce shut down			**0.85**	V
Fault Output Low Voltage	$V_{\overline{FLT}\_OUT\_LOW}$	$I_{\overline{FLT}}$ = 4mA			**0.4**	V
Sleep Mode: $\overline{SLEEP}$						
$\overline{SLEEP}$ High Voltage	$V_{\overline{SLEEP}\_HIGH}$	$R_{PULL-UP}$ = 1MΩ	**1.24**			V
$\overline{SLEEP}$ Sink Current	$I_{\overline{SLEEP}\_LOW}$	$\overline{SLEEP}$ active, $V_{\overline{SLEEP}}$ = 0.75V		60		µA
$\overline{SLEEP}$ Low Voltage	$V_{\overline{SLEEP}\_LOW}$	To externally induce shut down			**0.75**	V

Specified Operating Area

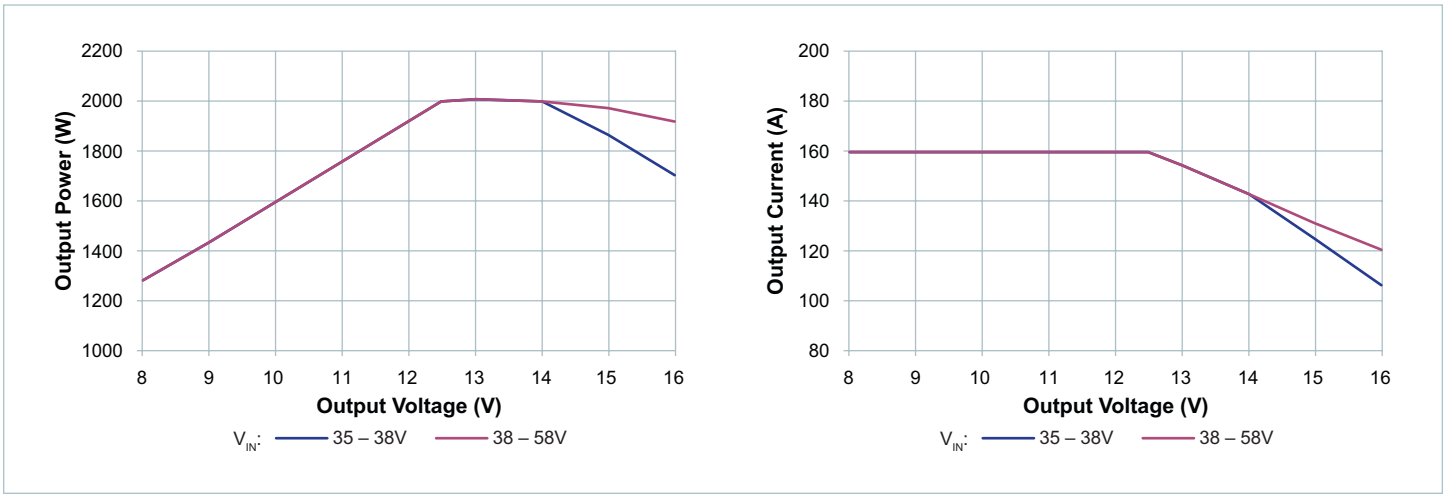


Figure 1 — *Specified electrical operating area; T_{CASE} = 25°C*

Thermal Specified Operating Area

The following figures present preliminary estimated performance data in a typical application environment.

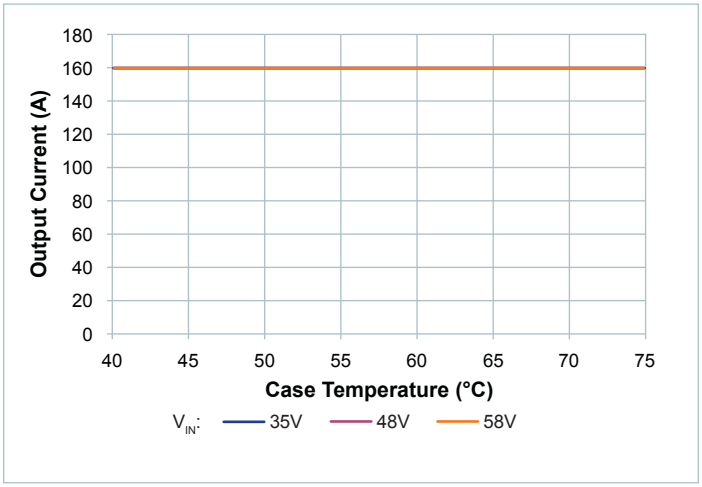


Figure 2 — *Thermal specified operating area at V_{OUT} = 8V: max system P_{OUT} vs. temperature, double-sided cooling*

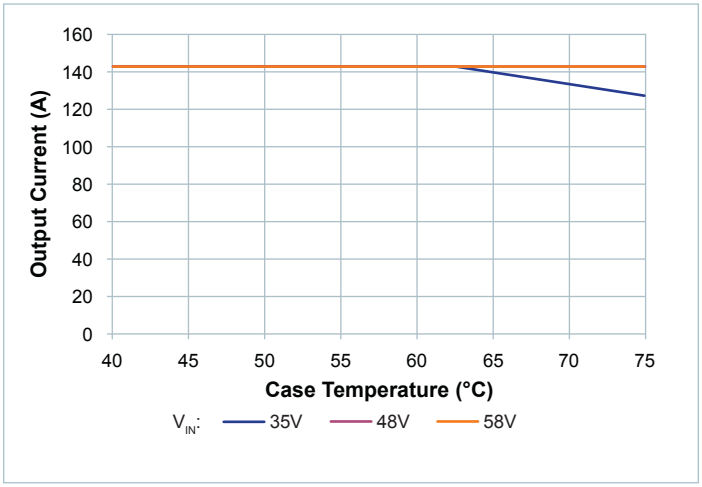


Figure 3 — *Thermal specified operating area at V_{OUT} = 14V: max system P_{OUT} vs. temperature, double-sided cooling*

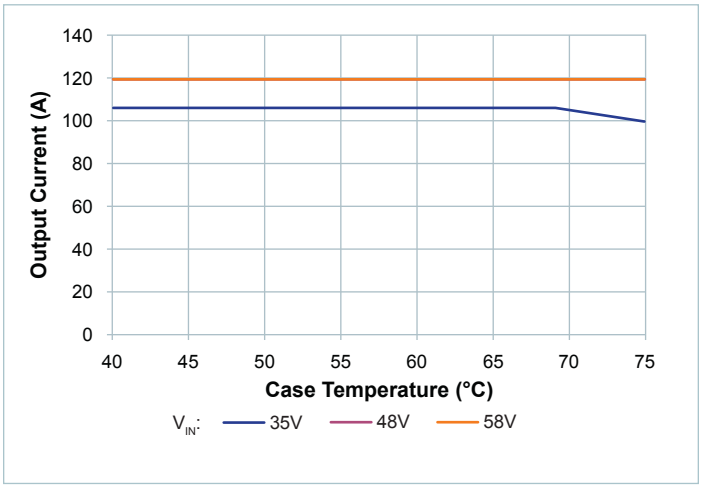


Figure 4 — *Thermal specified operating area at V_{OUT} = 16V: max system P_{OUT} vs. temperature, double-sided cooling*

Typical Performance Characteristics

The following figures present typical performance at T_C = 25°C, unless otherwise noted. See associated figures for general trend data.

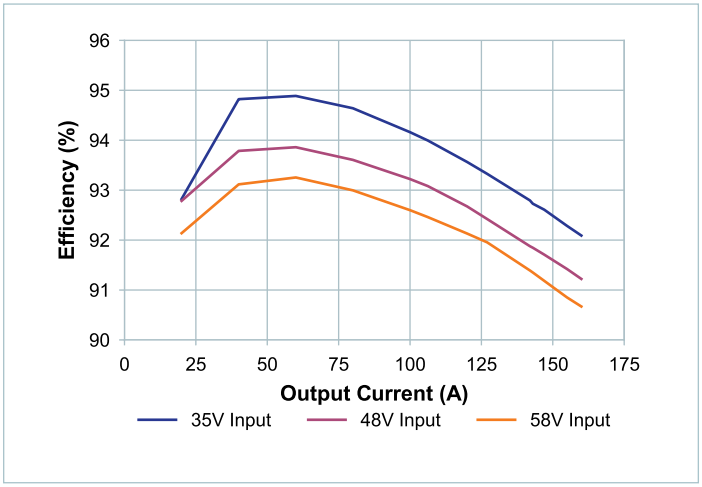


Figure 5 — *Efficiency at 25°C case temperature, V_{OUT} = 8V*

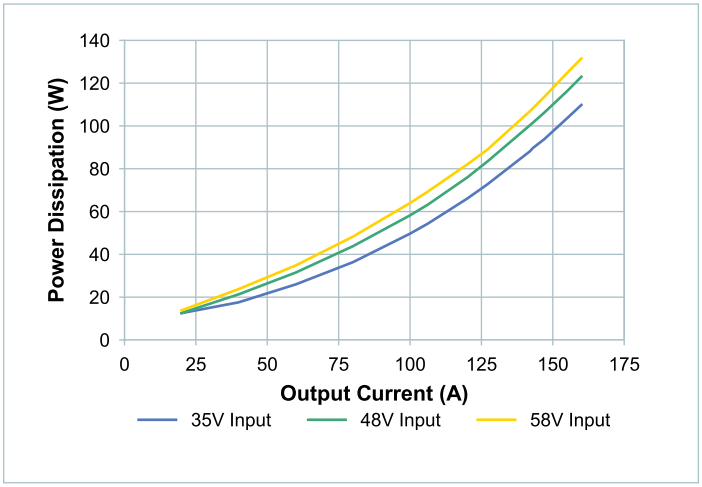


Figure 6 — *Power dissipation at 25°C case temperature, V_{OUT} = 8V*

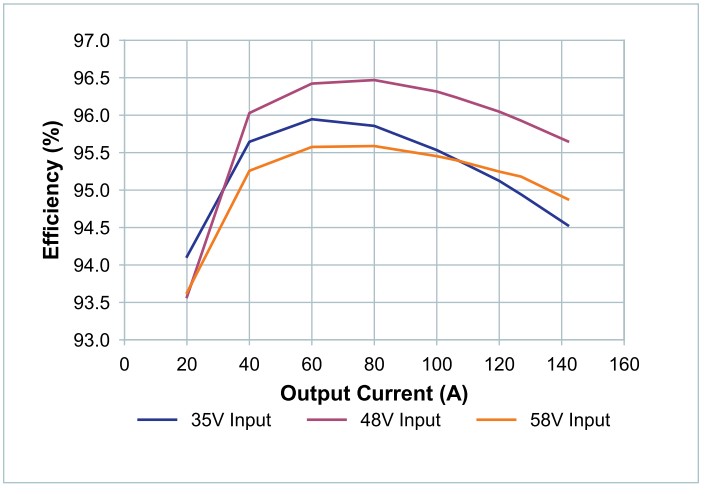


Figure 7 — *Efficiency at 25°C case temperature, V_{OUT} = 14V*

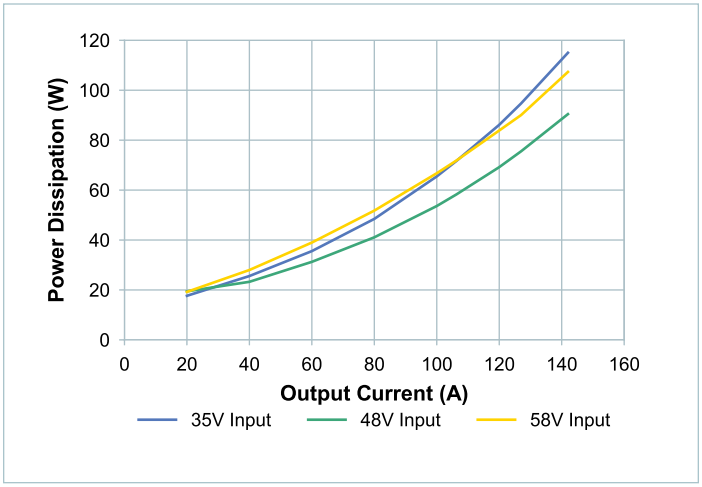


Figure 8 — *Power dissipation at 25°C case temperature, V_{OUT} = 14V*

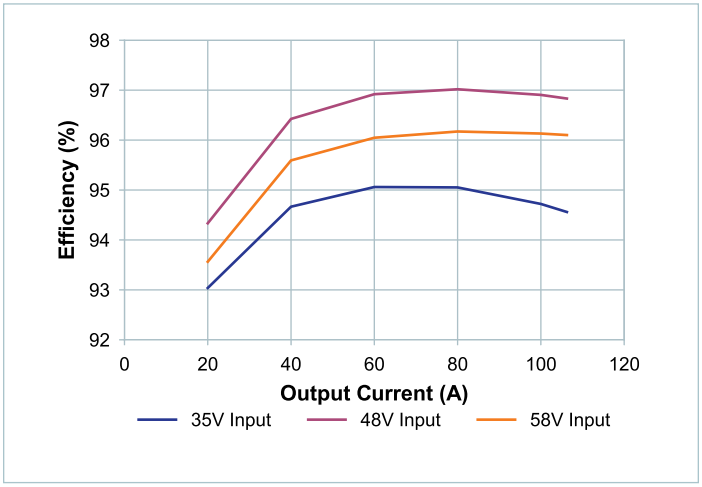


Figure 9 — *Efficiency at 25°C case temperature, V_{OUT} = 16V*

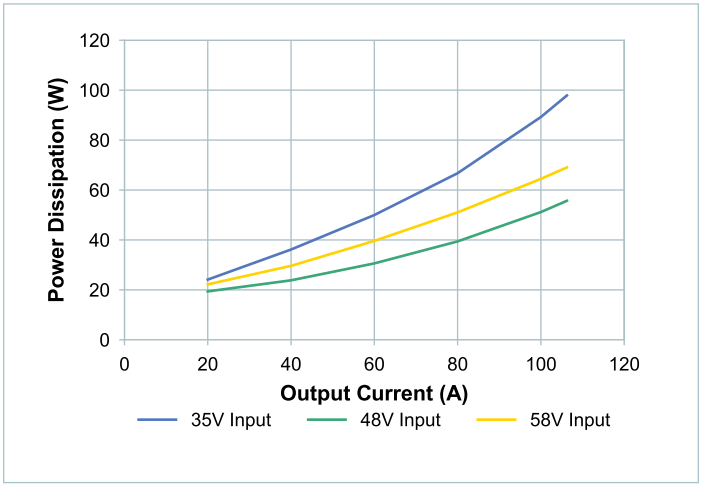


Figure 10 — *Power dissipation at 25°C case temperature, V_{OUT} = 16V*

Typical Performance Characteristics

The following figures present typical performance at T_C = 25°C, unless otherwise noted. See associated figures for general trend data.

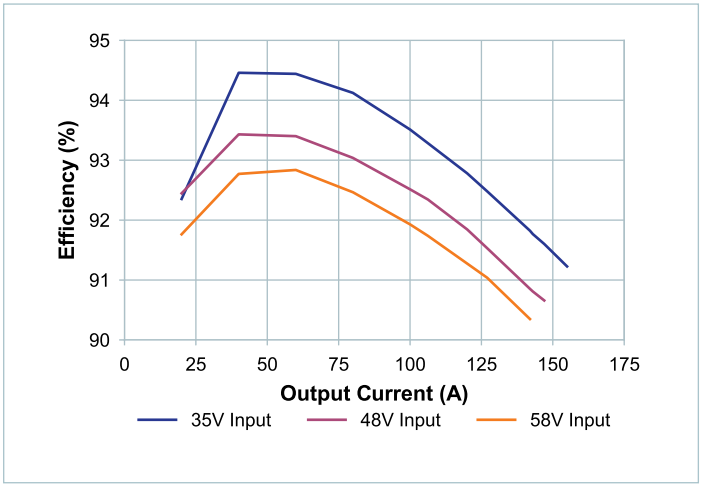


Figure 11 — *Efficiency at 75°C case temperature, V_{OUT} = 8V*

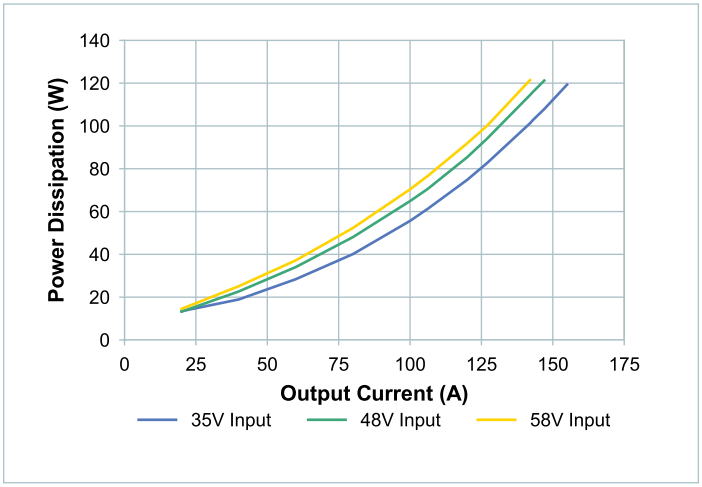


Figure 12 — *Power dissipation at 75°C case temperature, V_{OUT} = 8V*

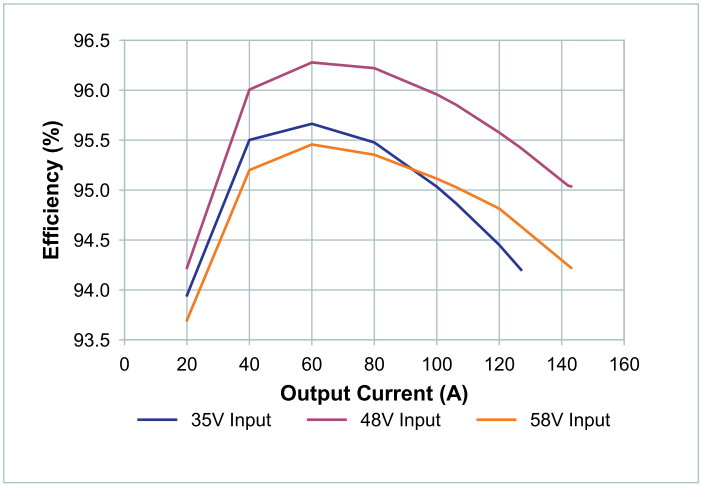


Figure 13 — *Efficiency at 75°C case temperature, V_{OUT} = 14V*

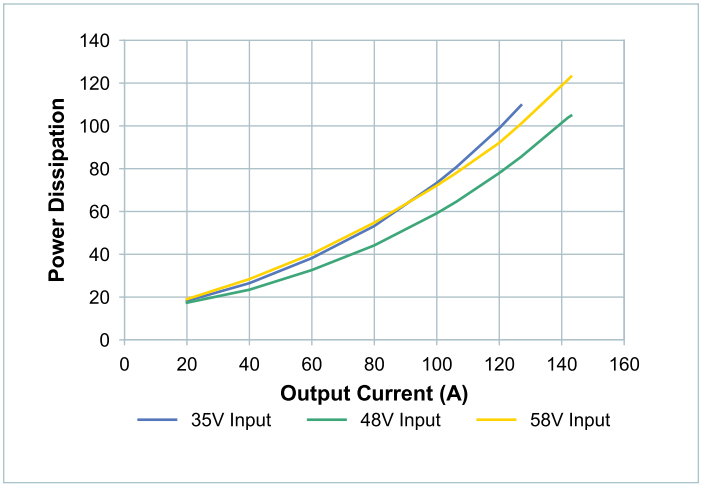


Figure 14 — *Power dissipation at 75°C case temperature, V_{OUT} = 14V*

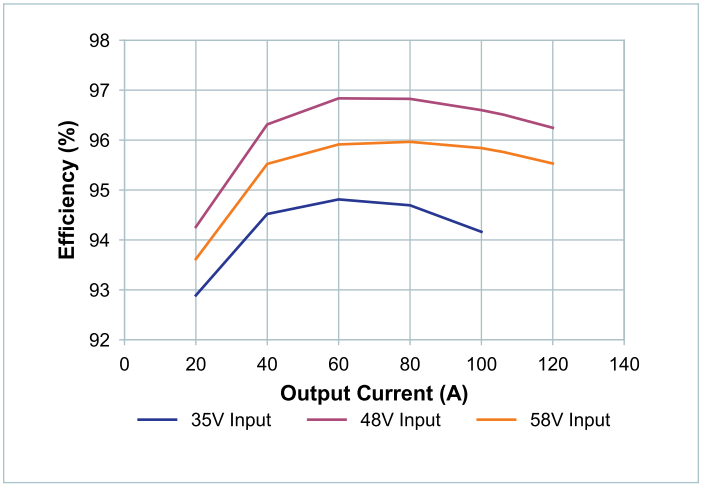


Figure 15 — *Efficiency at 75°C case temperature, V_{OUT} = 16V*

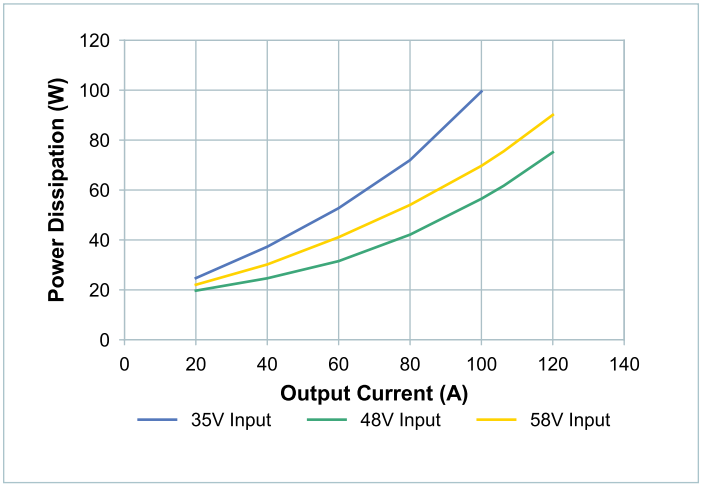


Figure 16 — *Power dissipation at 75°C case temperature, V_{OUT} = 16V*

Typical Performance Characteristics (Cont.)

The following figures present performance data in a typical application environment.

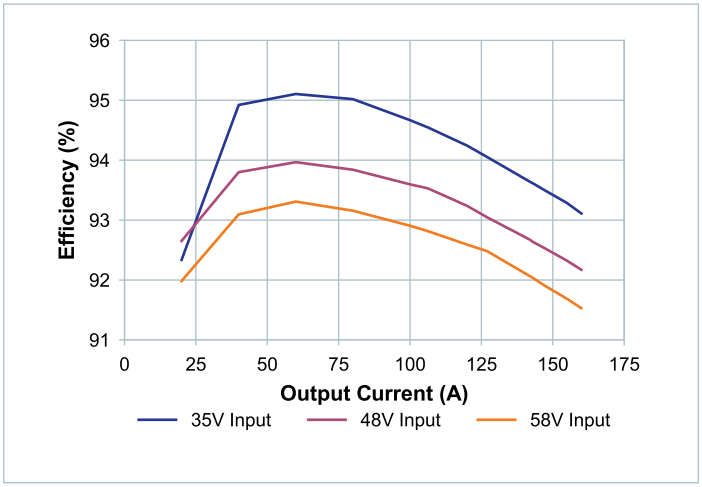


Figure 17 — *Efficiency at –40°C case temperature, V_{OUT} = 8V*

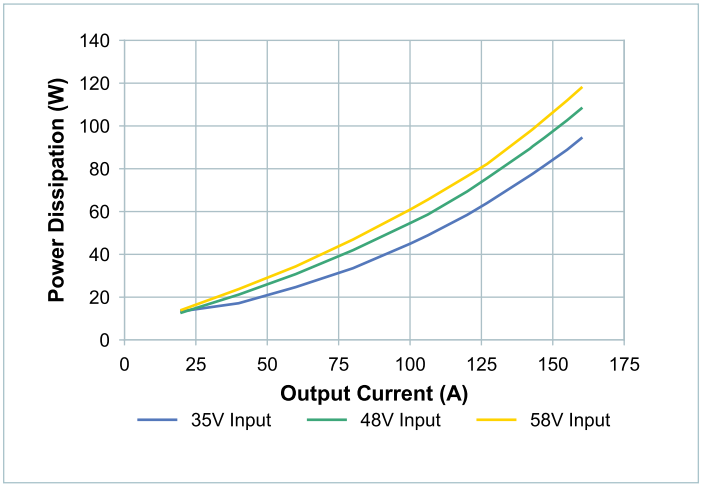


Figure 18 — *Power dissipation at –40°C case temperature, V_{OUT} = 8V*

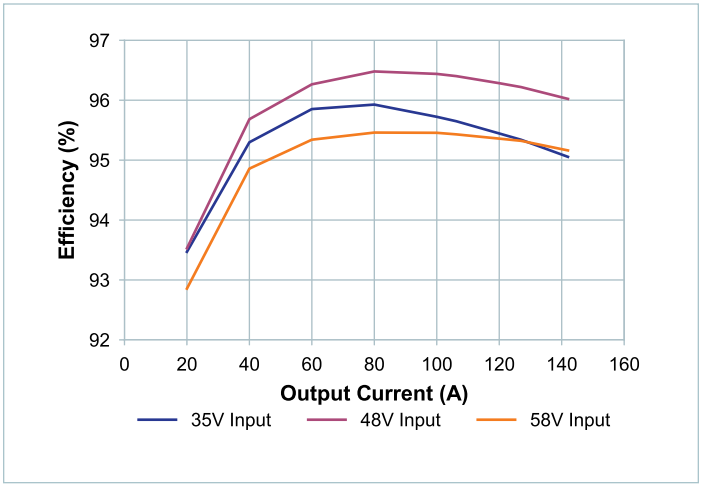


Figure 19 — *Efficiency at –40°C case temperature, V_{OUT} = 14V*

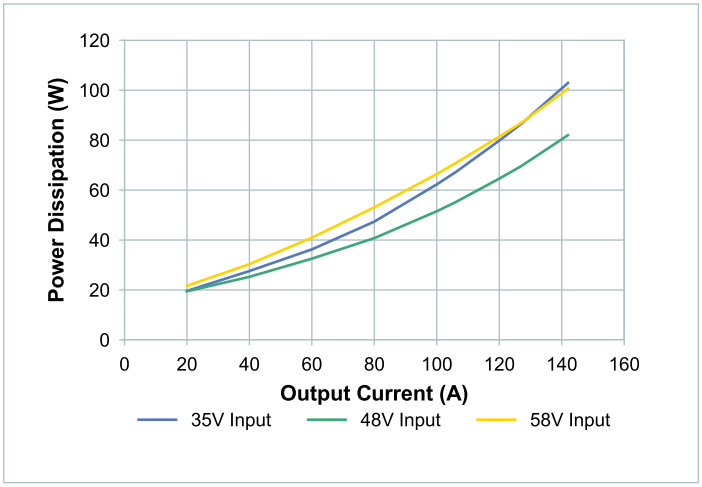


Figure 20 — *Power dissipation at –40°C case temperature, V_{OUT} = 14V*

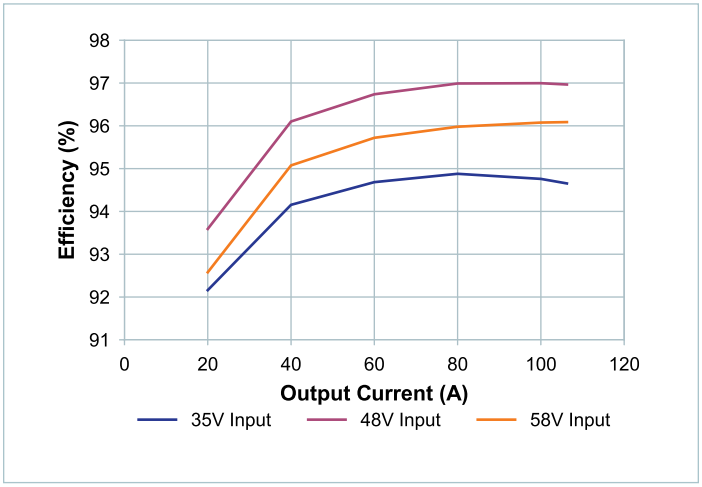


Figure 21 — *Efficiency at –40°C case temperature, V_{OUT} = 16V*

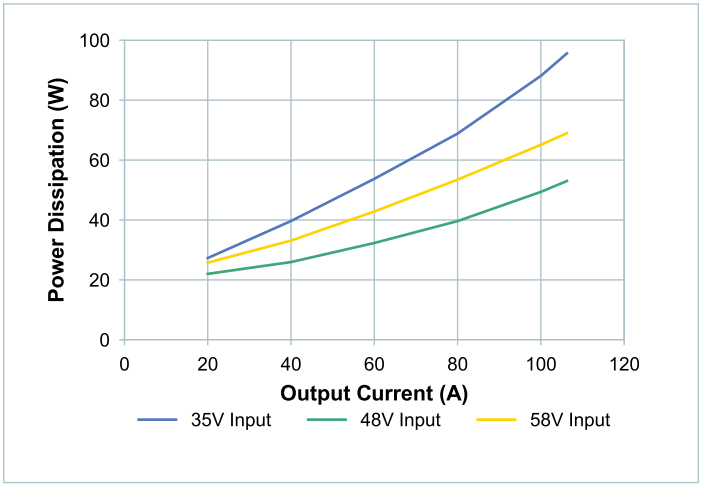


Figure 22 — *Power dissipation at –40°C case temperature, V_{OUT} = 16V*

Typical Performance Characteristics (Cont.)

The following figures present performance data in a typical application environment.

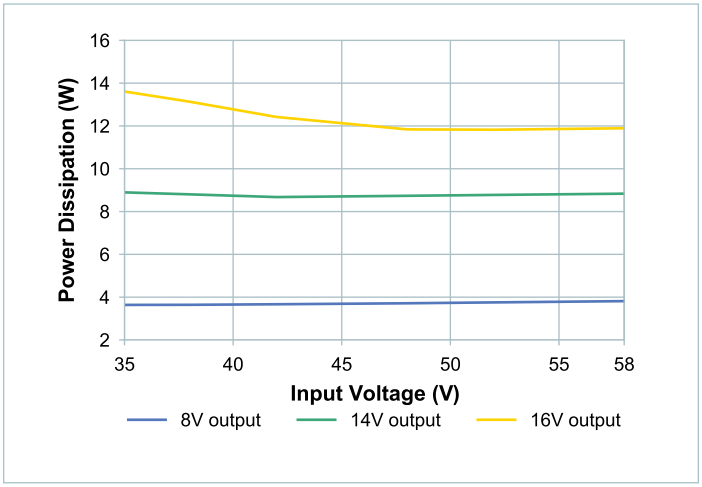


Figure 23 — *No-load power dissipation vs. line voltage, 25°C case temperature*

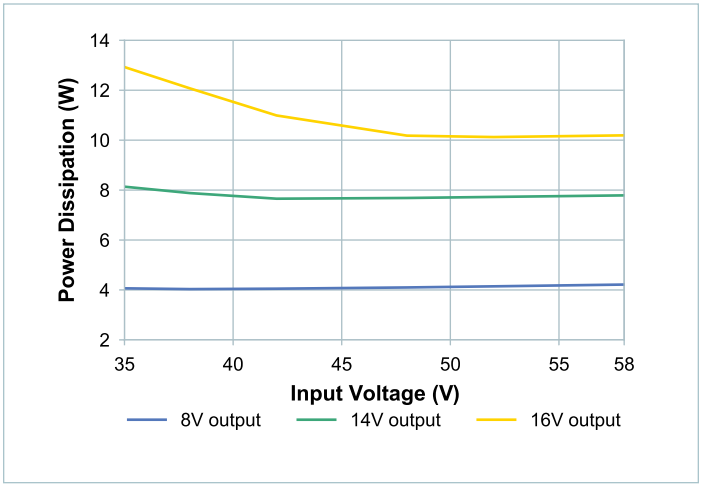


Figure 24 — *No-load power dissipation vs. line voltage, 75°C case temperature*

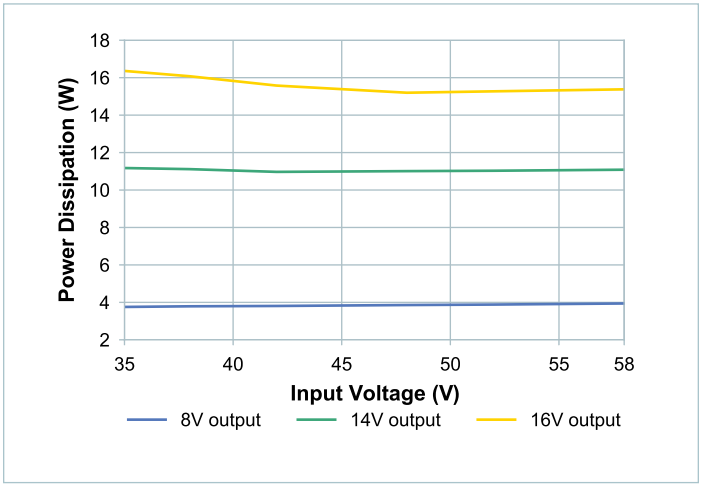


Figure 25 — *No-load power dissipation vs. line voltage, –40°C case temperature*

Terminal Descriptions

+IN – DCM Input Power

The +IN terminal is the power input to the regulation stage. External filtering and decoupling techniques are application-specific. Low-ESR ceramic capacitors are recommended between the DCM input and power ground.

PGND – Power Ground

The DCM is a three-terminal non-isolated regulator. PGND is the common power return for +IN and +OUT.

+OUT – DCM Output Power

The +OUT terminal is the power output from the current multiplication stage. External filtering and decoupling techniques are application-specific. Low-ESR ceramic capacitors are recommended between the DCM output and power ground.

+INV – DCM Intermediate Power Node

The +INV terminal is an intermediate power node between the regulation and current-multiplication powertrain stages.

EAO – Modulator Input

The EAO terminal provides access to the error amplifier output and is the control node input to the regulation stage, which determines the DCM output power.

EN – Enable

If the EN terminal is left floating or driven high, the DCM is enabled. When EN is pulled low, the DCM is disabled.

ADDR, SCL, SDA – PMBus® Interface Address, Serial Clock and Serial Data

Address is a multi-level analog input which sets the address at initial power-up.

Serial clock (SCL) and serial data (SDA) require external pull-up resistors for normal operation. Refer to System Management Bus (SMBus) Specification version 3.0 for details.

$\overline{FLT}$ – Fault Monitor

$\overline{FLT}$ is an open-drain terminal with an internal pull-up and indicates fault status. $\overline{FLT}$ is active-low, so when any fault protection is active the terminal will drive low. When the module is enabled and not in a fault condition, the terminal will pull high. The module monitors the status of this terminal, so if an external sub-circuit pulls $\overline{FLT}$ low, the module will also be disabled.

Note: $\overline{FLT}$ displayed as FLT* on the package drawing.

SYNCI – Factory Use Only

Leave SYNCI terminal floating.

IMON – Factory Use Only

Leave IMON terminal floating.

$\overline{SLEEP}$ – Sleep Mode Control

The $\overline{SLEEP}$ terminal is used to configure the unit into a high-impedance state at both the input and output power terminals for low quiescent power consumption. When held low, the internal bias generation and powertrain controller are fully disabled. When allowed to float, the internal bias-generation circuitry and powertrain controller are active.

The PMBus interface is inactive when the $\overline{SLEEP}$ terminal is held low.

Functional Description

The DCM3735 is a non-isolated, regulated DC-DC power converter with PMBus® control and telemetry, in a thermally adept package. It consists of a ZVS buck-boost first-stage block followed by a ZVS, ZCS Sine Amplitude Converter™ current multiplier second stage. The current multiplier operates at a fixed step-down ratio of 3, and so all regulation is performed by Stage 1. The output voltage sense for the regulation control loop is taken at the module output terminals after the current multiplier, for tight regulation accuracy. All PMBus output voltage set-point control and telemetry is provided by Stage 1.

The DCM offers peak current and power ratings that are generally 10% higher than the continuous ratings for up to 1ms for dynamic loads and higher transient requirements. The full peak load capability is available up to an output voltage set point of 12.5V. Above 12.5V the peak current rating is linearly reduced to avoid risk of shut down due to an overvoltage event, as shown in Figure 1.

DCM Power Up

When input voltage is applied, the DCM PMBus address is sensed and latched based on the pull-down resistor applied to the ADDR terminal. The address remains fixed until input voltage is removed.

DCM Start Up

Any time the DCM input voltage is within UVLO and OVLO, the DCM has not been disabled via the EN or $\overline{FLT}$ control terminals, and it has recovered from any previously occurring fault protections, it will attempt to start.

At start up, the $\overline{FLT}$ terminal goes inactive (high) and the Stage 2 current multiplier begins switching. Then the Stage 1 buck-boost regulator stage begins switching and its reference rises to generate the soft-start ramp of module output voltage. The module output is capable of full rated continuous output current during soft-start.

The DCM output voltage rise is monotonic during soft start into static loads, once V_{OUT} exceeds 2V, provided the module has been disabled for at least $t_{OFF\text{-}MONO}$. If the module restarts more quickly than $t_{OFF\text{-}MONO}$ then residual energy stored on the +INV node between the Stage 1 and Stage 2 powertrains can cause an output voltage transient to occur at the beginning of the soft-start ramp.

Pulse-Skip Mode (PSM)

The ZVS buck-boost stage features a hysteretic pulse-skipping mode. At light-load conditions, switching cycles can be skipped in order to significantly reduce gate-drive power and improve efficiency. The regulator will automatically enter and exit PSM based on load. Depending on line and trim operating conditions, as well as capacitor and other component values, PSM may result in occasional skipping of one or many switching cycles.

Variable-Frequency Operation

The ZVS buck-boost stage is pre-programmed to a fixed, maximum base operating frequency. The maximum processed power determines the base frequency and associated power inductor with respect to other constraints to achieve peak efficiency at nominal operation. The operating frequency can be reduced from the base frequency as needed to maintain rated power capability at certain line voltage, trim voltage and load conditions. By reducing the operating frequency, or stretching the period of each switching cycle, the ZVS operation is preserved throughout the input line voltage range maintaining optimum efficiency. The current multiplication stage also exhibits variable frequency operation, though over a smaller frequency range relative to that of the ZVS buck-boost stage.

DCM Fault Response

If the DCM detects a fault, it pulls the $\overline{FLT}$ terminal low within t_{FAULT} and the powertrain stops at the end of the current switching cycle. Once the Fault Recovery Time ($t_{FAULT1\text{-}RECOVERY}$ or $t_{FAULT2\text{-}RECOVERY}$) elapses and the fault is no longer present, the DCM resumes operation according to EAO.

Input undervoltage, input overvoltage, overtemperature, EN or $\overline{FLT}$ terminals low, and output overvoltage faults are all level sensitive. The DCM will not attempt to start again after shut down as long as the fault is present, and will hold $\overline{FLT}$ low continuously. Note that $\overline{FLT}$ being held (externally) low will also inhibit restart of the DCM.

Other fault types like output voltage negative, output overcurrent or EAO_OVERLOAD can normally only occur when the module is operating. After shut down due to one of these faults, the DCM will attempt a restart after the specified fault recovery time, but may shut down repeatedly for as long the fault condition persists.

Input Undervoltage Recovery and Lockout Thresholds (V_{IN_UVLO+} and $V_{IN\_UVLO\_HYS}$)

The DCM monitors the +IN terminal. It will not start until the input voltage exceeds the undervoltage recovery threshold (V_{IN_UVLO+}) and will shut down if the input voltage crosses below this threshold by more than the undervoltage lockout hysteresis ($V_{IN\_UVLO\_HYS}$).

A V_{IN_UVLO} event will set byte 3, bit 3 in the MFR_STATUS_FAULTS (F0h) status register, as well as byte 2, bit 0 FLT_FALLING_EDGE.

Input Overvoltage Lockout and Recovery Thresholds (V_{IN_OVLO+} and $V_{IN\_OVLO\_HYS}$)

If the input voltage rises above the overvoltage lockout threshold (V_{IN_OVLO+}), the DCM will shut down. The DCM will attempt to recover once the input voltage has reduced below this threshold by at least the overvoltage lockout hysteresis ($V_{IN\_OVLO\_HYS}$).

A V_{IN_OVLO} event will set byte 3, bit 4 in the MFR_STATUS_FAULTS (F0h) status register, as well as byte 2, bit 0 FLT_FALLING_EDGE.

Overtemperature Fault Threshold (T_{OT})

The DCM features an overtemperature shut down, which is designed to protect against catastrophic failure due to excessive temperatures. The overtemperature shut down cannot be used to ensure the device stays within the recommended operating temperature range, because the overtemperature threshold T_{OT} engages at or above the maximum rated temperature. When overtemperature shut down occurs, the DCM stops processing power and $\overline{FLT}$ drives low. The DCM will restart after the temperature has decreased below T_{OT} by at least the overtemperature restart hysteresis, T_{OT_HYS}.

If the overtemperature fault threshold is exceeded, byte 1, bit 0 in the MFR_STATUS_FAULTS (F0h) status register will be set. Unlike other faults, the Overtemperature Fault will not set byte 2, bit 0 FLT_FALLING_EDGE due to how the overtemperature condition is sensed.

Output Undervoltage (V_{OUT_UVP})

When the DCM operates as a constant current source, the output voltage must decline in order to maintain the set current trim at higher load conditions. The DCM will shut down if the output voltage declines below the UVP threshold, V_{OUT_UVP}.

A V_{OUT_UVP} fault will set byte 1, bit 2 in the MFR_STATUS_FAULTS (F0h) status register as well as byte 2, bit 0 FLT_FALLING_EDGE.

Output Overvoltage Threshold (V_{OUT_OVP})

The DCM will shut down if the voltage at +INV rises above the OVP threshold, V_{OUT_OVP}. The sense point is taken before the second stage current multiplier, so the effective output referred threshold depends on the voltage drop across the second stage. The DCM will restart after the recovery time $t_{FAULT2\_RECOVERY}$.

A V_{OUT_OVP} fault can also be produced by the ZVS buck-boost stage. If the buck-boost produces the OVP event, the DCM will restart after the recovery time $t_{FAULT1\_RECOVERY}$.

A V_{OUT_OVP} fault will set byte 3, bit 5 in the MFR_STATUS_FAULTS (F0h) status register, as well as byte 1, bit 0 FLT_FALLING_EDGE.

Output Voltage Negative (V_{OUT_NEG})

When the DCM output voltage is higher than $V_{OUT\_NEG\_RE\text{-}ARM}$, the Output Voltage Negative fault is armed. Once armed, if the DCM output voltage becomes reverse-biased by more than V_{OUT_NEG}, it will shut down and stop processing power. It will also set byte 3, bit 6 in the MFR_STATUS_FAULTS (F0h) status register, as well as byte 2, bit 0 FLT_FALLING_EDGE.

This can occur if the module is disabled or shuts down due to another fault, and either the load is inductive and brings V_{OUT} below ground, or if the DCM output is connected to a downstream load such as a VTM which sinks current, which can generate a negative voltage bias on the DCM output terminal.

When the DCM is disabled via EN, or has shut down due to any fault type, the Output Voltage Negative fault is blanked from further activation until the output voltage again exceeds $V_{OUT\_NEG\_RE\text{-}ARM}$. This permits the DCM to be easily restarted even when a negative V_{OUT} condition persists (as may be the case with a downstream current sink present, like an active VTM powertrain).

EAO Overload (V_{EAO_OL} and t_{EAO_OL})

EAO, the control input voltage to the internal modulator, is driven by the internal error amplifier closing the module control loop. The voltage on this terminal varies according to the input voltage, the output trim setting and the load condition.

In cases where the DCM cannot support a load at a given input voltage and trim setting and the voltage on the EAO terminal exceeds the specified EAO overload threshold (V_{EAO_OL}), the overload timer starts. If this condition persists for longer than t_{EAO_OL}, the $\overline{FLT}$ terminal is asserted low and the unit will shut down.

An EAO overload fault will set byte 2, bit 1 in the MFR_STATUS_FAULTS (F0h) status register as well as byte 2, bit 0 FLT_FALLING_EDGE.

EAIN High (EAIN_HI)

When operating multiple DCMs in an array, the EAO terminal is interconnected between units in order to facilitate accurate current sharing. If the output voltage trim setting is not identical among units then it is possible that the output voltage sensed by the error amplifier is too high for the compensation.

If the EAO amplifier reference voltage is 120% of the expected reference voltage, the unit will shut down and an EAIN_HI fault will occur.

An EAIN high fault will set byte 2, bit 5 in the MFR_STATUS_FAULTS (F0h) status register as well as byte 2, bit 0 FLT_FALLING_EDGE.

Note: At higher output voltage set points, the fault may be reported as V_{OUT_OVP}.

Overcurrent Threshold (I_{OC})

The DCM output current is continuously measured during operation, and if it exceeds the overcurrent shut-down threshold (I_{OC}), for longer than overcurrent timeout (t_{IOC}), the DCM will shut down and $\overline{FLT}$ is driven low. The overcurrent is monitored by both the current multiplier stage and the buck-boost regulation stage. If the buck-boost stage detects the overcurrent (I_{OC1}), then the MFR_STATUS_FAULTS bits VOUT_NEG or Q3_SIL may set. If only the current multiplier stage detects the fault (I_{OC2}), then only the FLT terminal falling edge will be set. Any of these bits indicate the presence of an overcurrent condition. The DCM will restart after the recovery time $t_{FAULT1\_RECOVERY}$ or $t_{FAULT2\_RECOVERY}$ depending on which powertrain stage shut down.

Short Circuit Detection (I_{SHORT})

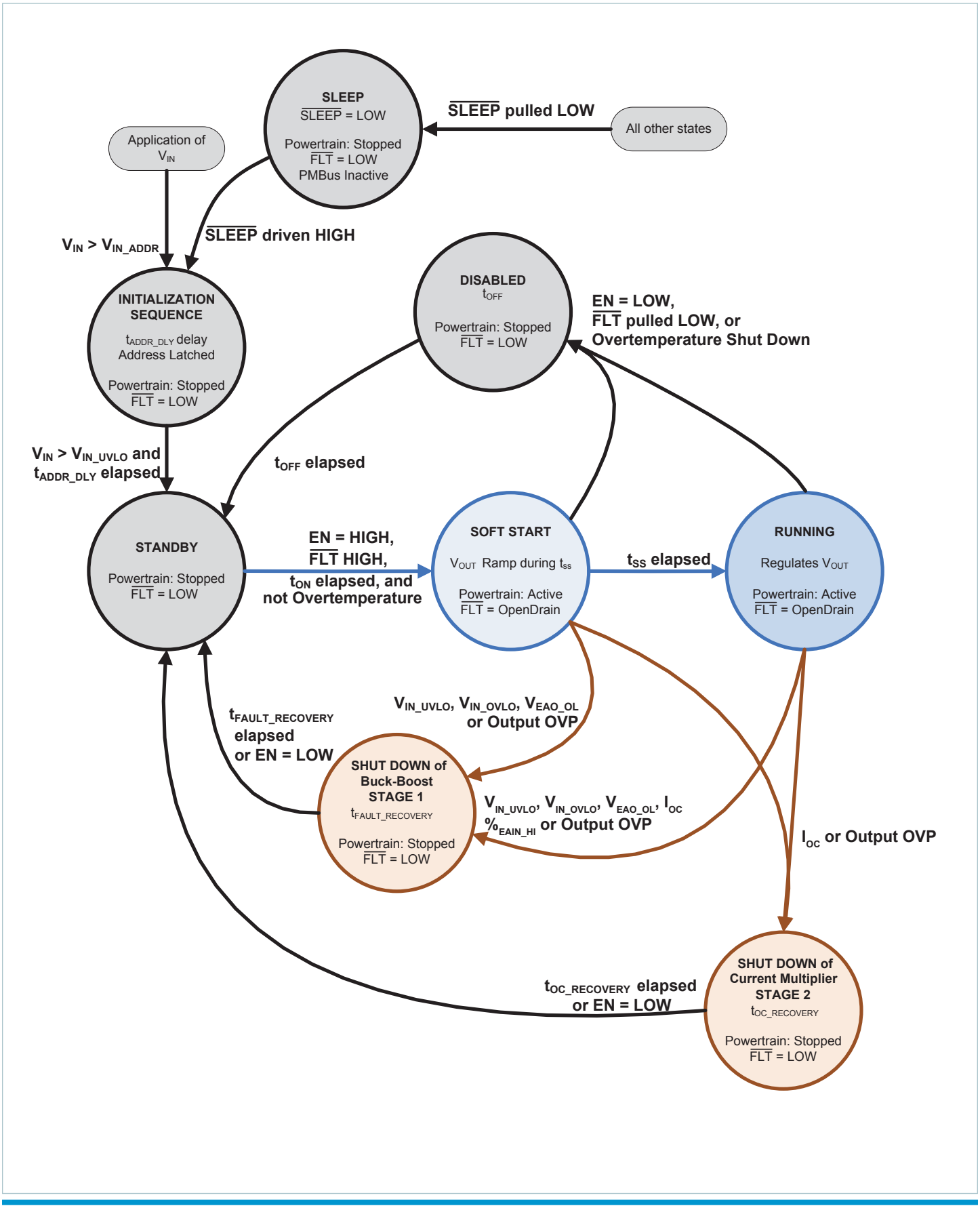
In the event of a short circuit occurring during operation or during start up, the DCM fast short-circuit detection will shut down the powertrain and drive $\overline{FLT}$ low. The MFR_STATUS_FAULTS bits Q1_FIL or Q3_FIL should set. The V_{OUT_NEG} may also set. The DCM will restart after the recovery time $t_{FAULT1\_RECOVERY}$ or $t_{FAULT2\_RECOVERY}$, depending on which powertrain stage shut down. For the case where the short-circuit condition occurs while the DCM is running, the $\overline{FLT}$ line will be asserted after t_{FAULT}.

$\overline{FLT}$ Fault

If the $\overline{FLT}$ terminal is pulled low, the unit will shut down in the same manner as other faults listed here. Byte 2, bit 0 FLT_FALLING_EDGE bit will be set in the MFR_STATUS_FAULTS (F0h) status register.

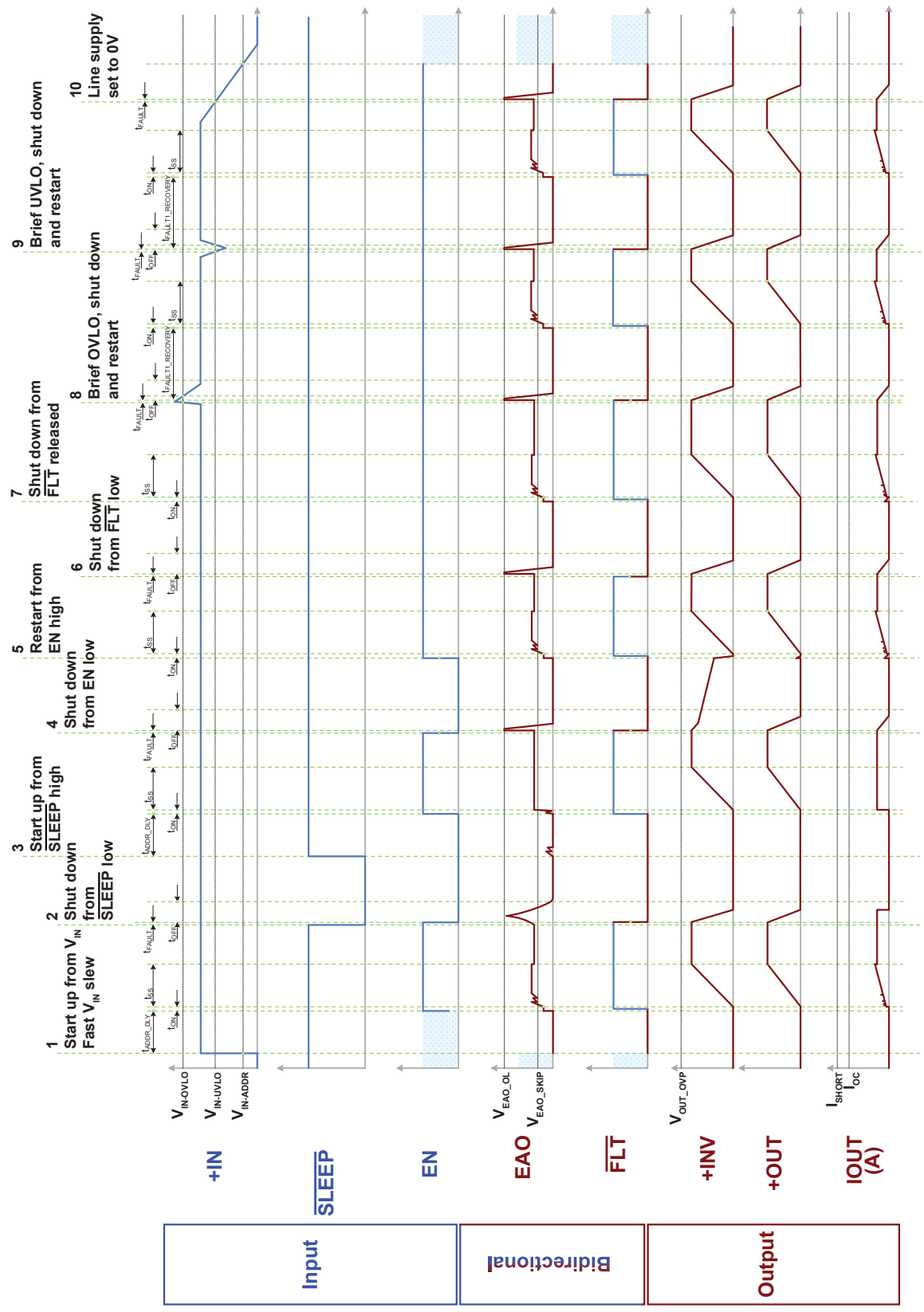
High-Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



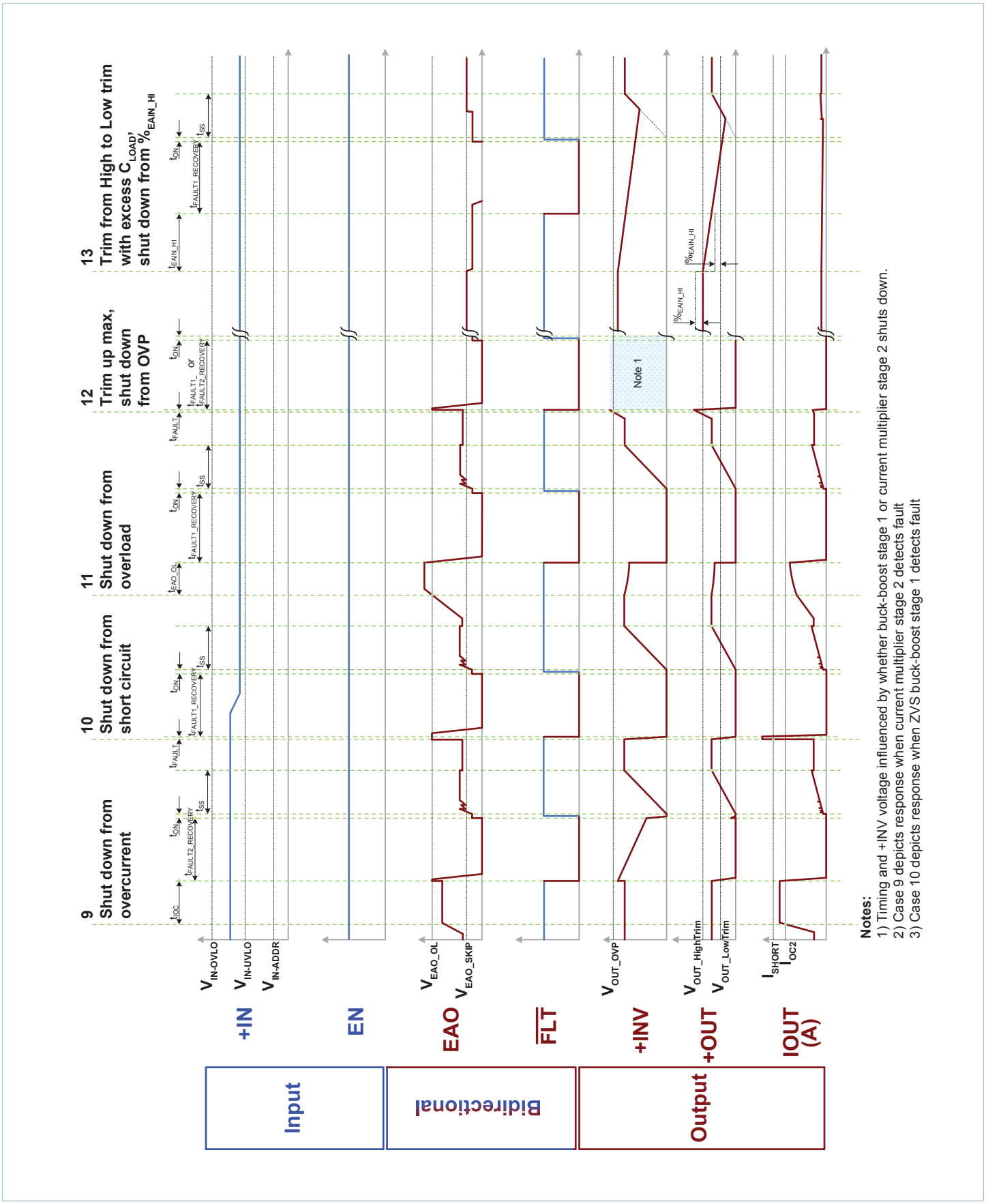
Timing Diagrams

Module inputs are shown in blue; module outputs are shown in brown.



Timing Diagrams (Cont.)

Module inputs are shown in blue; module outputs are shown in brown.



Design Guidelines

Input Filter Stability

Regulating switch-mode power supplies like the DCM present a negative impedance to the voltage source that is powering them. To ensure stability of the regulation loop, the source impedance and the parasitic resistance and inductance of the interconnect lines must be considered. The high performance ceramic decoupling capacitors placed locally to the input to the DCM are effective in controlling reflected ripple current at the switching frequency. However their low ESR means they will not significantly damp an excessively high impedance of an upstream voltage source.

The regulator dynamic input impedance magnitude r_{EQ_IN} can be calculated by dividing the lowest line voltage by the full load input current. To ensure stability, two cases must be considered.

Input Filter case 1; inductive source and local, external, input decoupling capacitance with negligible ESR (i.e., ceramic type)

The voltage source impedance can be modeled as a series R_{LINE} L_{LINE} circuit. In order to guarantee stability the following conditions must be verified:

$$R_{LINE} > \frac{L_{LINE}}{(C_{IN} + C_{IN\_EXT}) \bullet \left| r_{EQ\_IN} \right|} \quad (1)$$

$$R_{LINE} << \left| r_{EQ\_IN} \right| \quad (2)$$

Notice that the local high-performance ceramic input capacitors should be included for this purpose. Equation 2 means that the line source impedance should be <10% of the regulator dynamic input resistance r_{EQ_IN}. for best performance, but the line source impedance must <50% of r_{EQ_IN}. However, R_{LINE} cannot be made arbitrarily low otherwise Equation 1 is violated and the system will show instability, due to under-damped RLC input network.

Input Filter case 2; inductive source and internal, external input decoupling capacitance with significant $R_{C_{IN\_EXT}}$ ESR (i.e., electrolytic type)

In order to simplify the analysis in this case, the input source impedance can be modeled as a simple inductor L_{LINE}. Notice that, the internal high-performance ceramic capacitors C_{IN} directly at the input of the DCM should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$\left| r_{EQ\_IN} \right| > R_{C_{IN\_EXT}} \quad (3)$$

$$\frac{L_{LINE}}{(C_{IN\_EXT} \bullet R_{C_{IN\_EXT}})} < \left| r_{EQ\_IN} \right| \quad (4)$$

Equation 4 shows that if the aggregate ESR is too small – for example by using only high-Q ceramic input capacitors (C_{IN_EXT}) – the system will be under-damped and may not be stable. As with Equation 2 above, a decade of margin in satisfying Equation 3 is preferred, but an octave of margin is considered the minimum.

Additional information can be found in the filter design application note AN:023. Lastly, consider the DCM maximum input voltage slew rate dV_{IN}/dt, which is needed to prevent overstress to input stage components in the module. Additional circuitry may be required at the DCM input if the filter solution can exceed that slew rate.

Input Fuse Recommendations

A fuse should be incorporated at the input to the DCM, in series with the +IN terminal. An 80A or smaller input fuse (Littelfuse® Nano²® 881F Series) is required to comply with safety agency conditions of acceptability. Always ascertain and observe the safety, regulatory, or other agency specifications that apply to your specific application.

Thermal Design

Thermal management of DCM internal power dissipation is critical to reliable operation, and ample cooling is preferred since efficiency and reliability are better at lower internal temperatures. Figure 26 shows a thermal impedance model that can be used to estimate the maximum temperature of the hottest internal component for a given electrical and thermal operating condition.

The circuit model assumes each of those areas identified as thermal boundaries are isothermal although not necessarily the same temperature as the other boundary areas. Use of non-conductive TIM (Thermal Interface Material) is required to prevent shorting conductive surfaces on the module case.

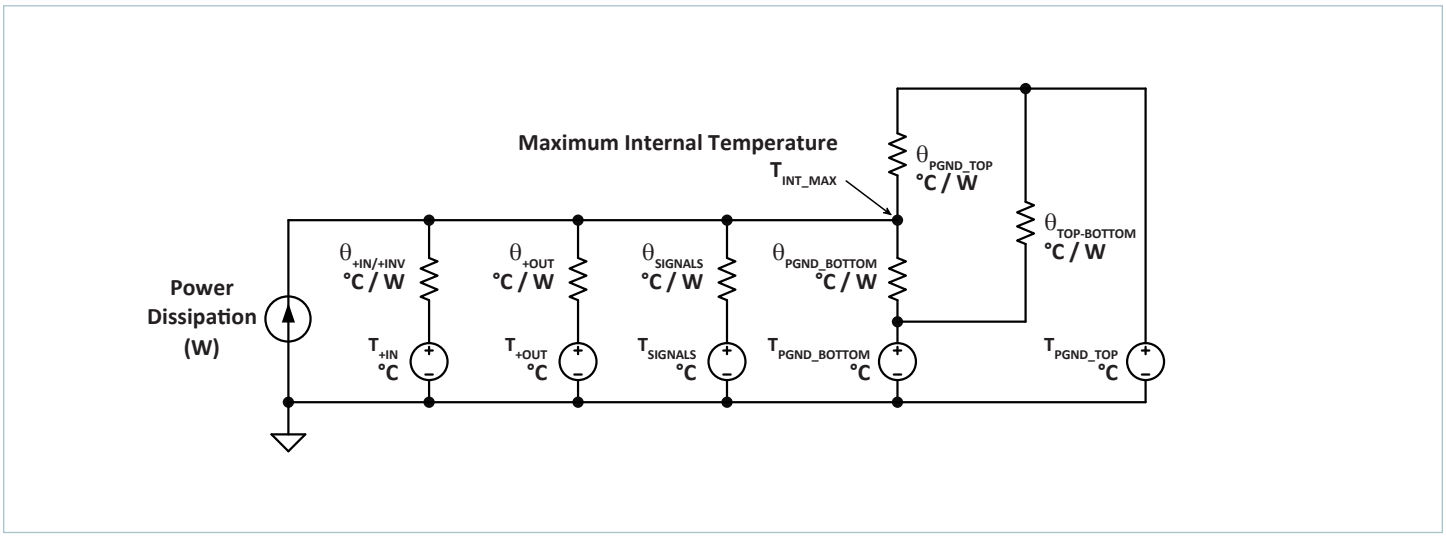


Figure 26 — *Thermal model*

Symbol	Thermal Impedance (°C / W)	Definition of Estimated Thermal Resistance
θ_{PGND_TOP}	0.85	From top of PGND terminal to maximum temperature internal component
$\theta_{+IN/+INV}$	16	From +IN/+INV terminal to maximum temperature internal component
θ_{+OUT}	8.4	From +OUT terminal to maximum temperature internal component
$\theta_{SIGNALS}$	19	From collective signal terminals to maximum temperature internal component
θ_{PGND_BOTTOM}	1.0	From bottom of PGND terminal to maximum temperature internal component
$\theta_{TOP-BOTTOM}$	3.9	From PGND_TOP to PGND_BOTTOM

Table 1 — *Preliminary thermal impedances*

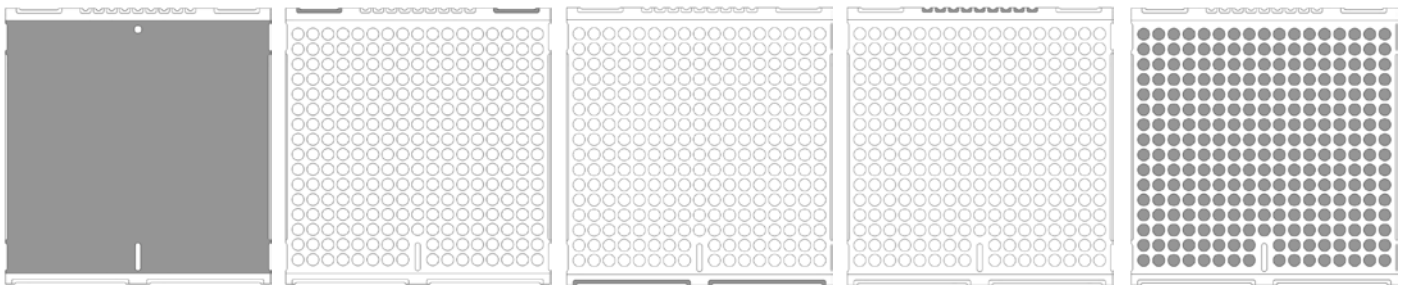


Figure 27 — *Thermal model boundary conditions; area defined as shaded*

Thermal Design — Typical Performance

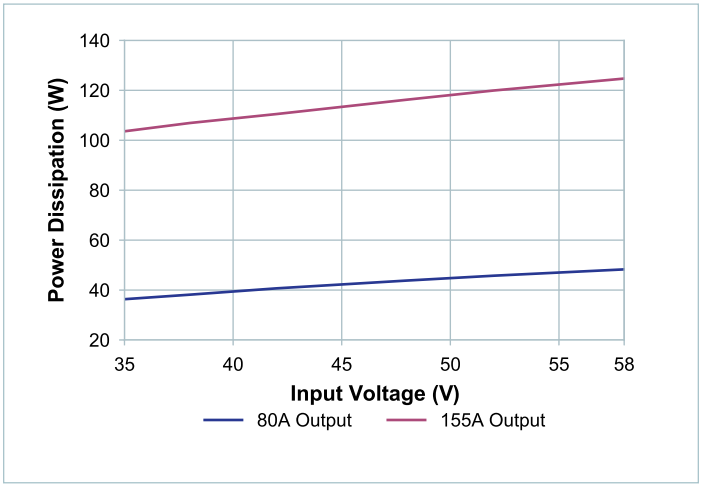


Figure 28 — *Power dissipation vs. line voltage, V_{OUT} = 8V, at 25°C case temperature*

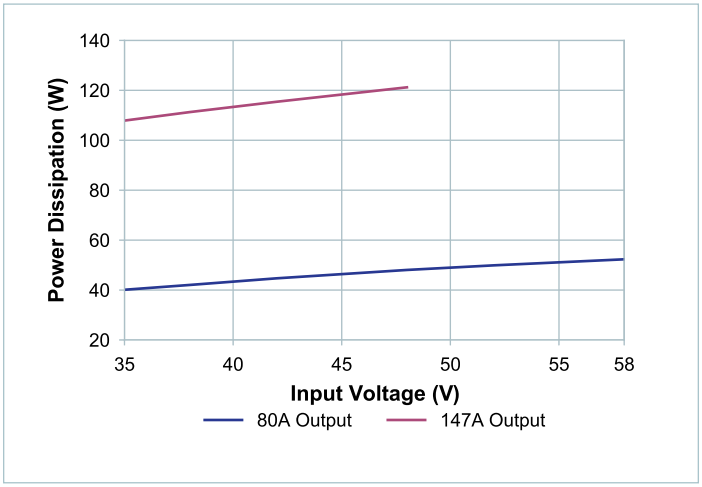


Figure 29 — *Power dissipation vs. line voltage, V_{OUT} = 8V, at 75°C case temperature*

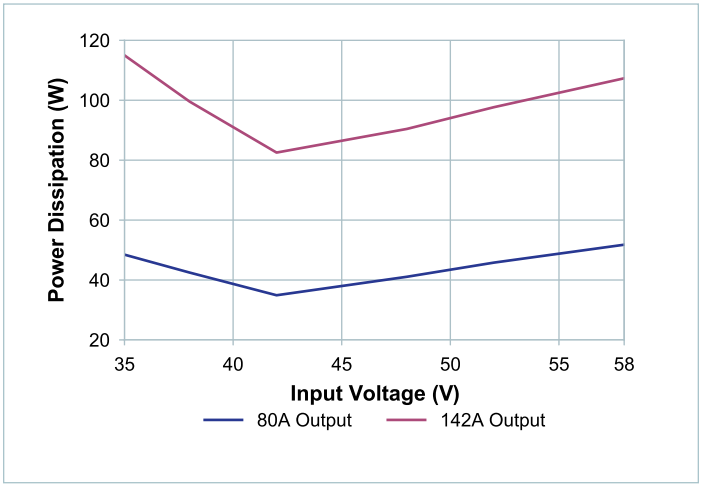


Figure 30 — *Power dissipation vs. line voltage, V_{OUT} = 14V, at 25°C case temperature*

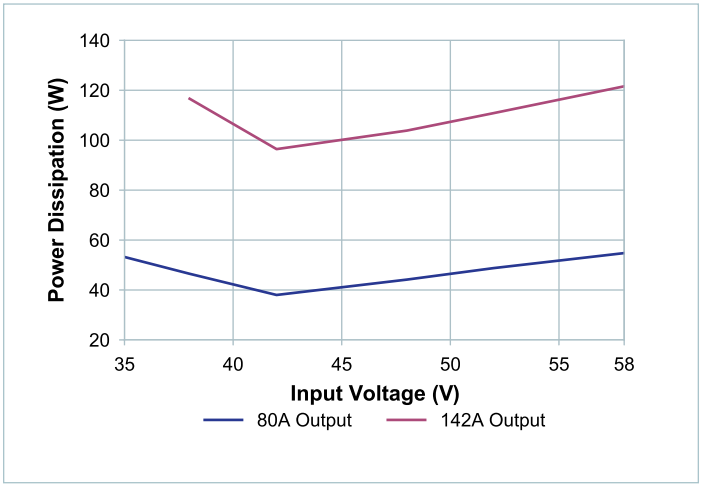


Figure 31 — *Power dissipation vs. line voltage, V_{OUT} = 14V, at 75°C case temperature*

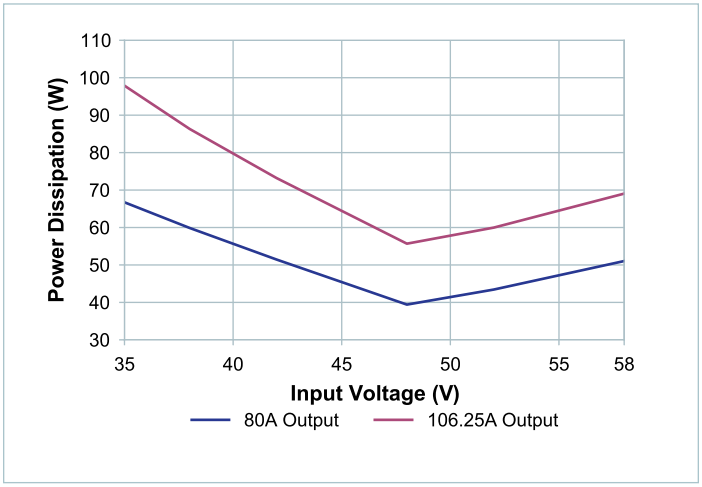


Figure 32 — *Power dissipation vs. line voltage, V_{OUT} = 16V, at 25°C case temperature*

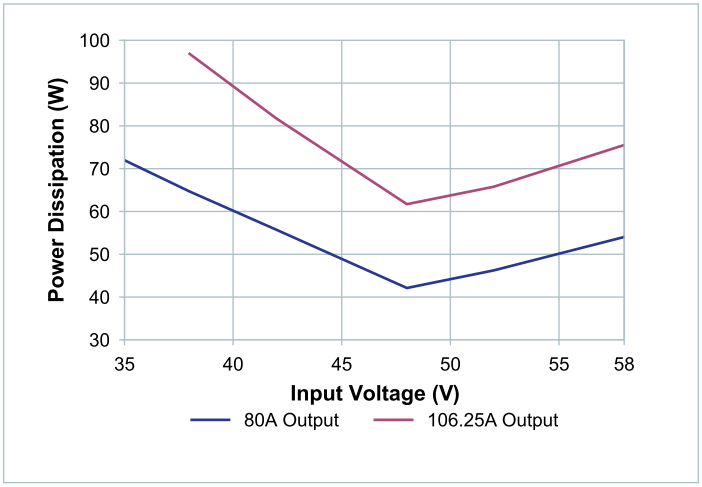


Figure 33 — *Power dissipation vs. line voltage, V_{OUT} = 16V, at 75°C case temperature*

Additional PCB Layout Considerations

DCM output capacitance is needed to bypass the high-frequency ripple at its source. The amount of capacitance varies by design and should be distributed as shown in the diagram.

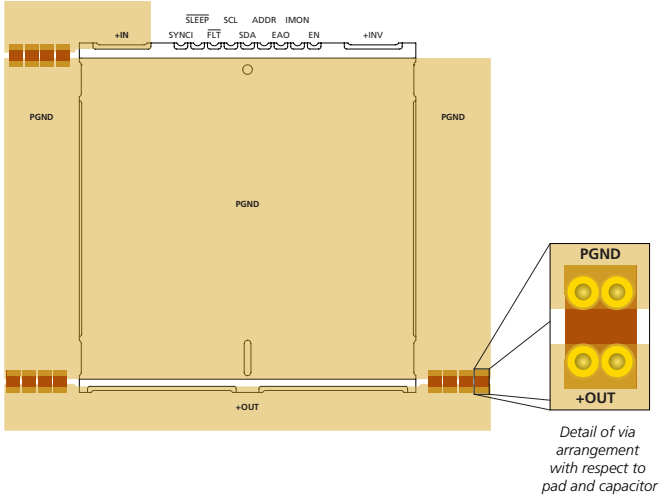


Figure 34 — *Recommended positioning of external capacitance relative to +IN, +OUT and PGND terminals*

The mechanical drawings in later sections include the recommended land pattern to use when creating a PCB footprint. The recommend footprint pad is intentionally narrower than the actual product terminal. This allows room for the pick-and-place machine worst-case placement tolerances. The worst case is a package terminal exactly aligned with the inner edges of footprint pad.

If the product is water washed post assembly, then the PGND circular thermal pads under the product must be copper-defined.

If no-clean solder flux is used during assembly, then PGND thermal pad apertures may be solder-mask-defined.

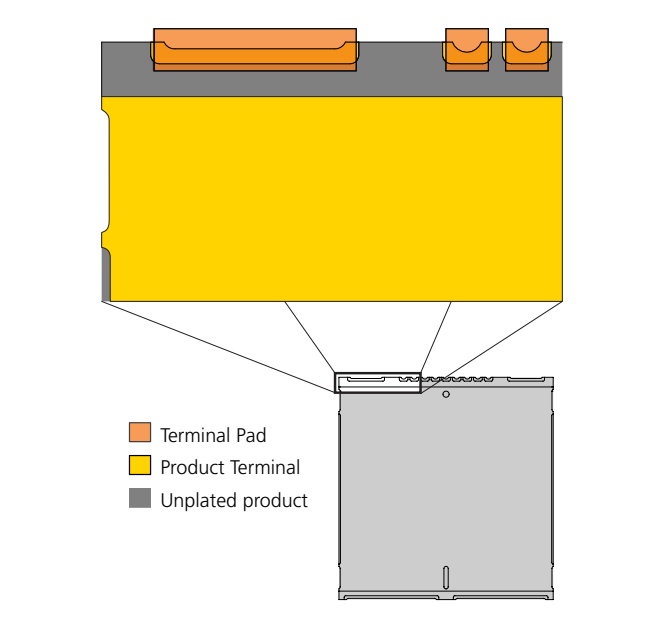


Figure 35 — *Product drawing vs. recommended land pattern*

Parallel Operation for High-Power Arrays

Loads that exceed the rated current or power of a single DCM can be powered by an array of DCMs, with array sizes up to n_{ARRAY} max modules. A properly configured array of n DCMs provides the rated power or current of a single module times n, with no electrical de-rating required.

At the schematic level, a DCM array is configured by setting a unique address for each DCM and directly interconnecting the control terminals: EN, $\overline{FLT}$, SDA and SCL. Additionally, all EAO terminals must be interconnected.

For power connections in an array, each DCM should still have dedicated multi-layer chip capacitors at the input and output. The DCM +OUT terminals must be directly connected together. The DCM +IN terminals are not directly connected, but instead each has its own dedicated fuse and input filter. The fuse and filter of each DCM in the array must be powered from the same voltage source; different input voltages are not permitted.

The DCMs should be placed in close proximity so that interconnected control signals can be short, which reduces stray capacitance and pickup of noise. However, DCMs must still be separated sufficiently to permit adequate cooling to avoid excess internal temperatures. If the PCB provides the dominant cooling path for heat to flow from the modules, physical separation of modules becomes more important. PGND should be carried on contiguous plane layers to optimize effectiveness of high-frequency bypassing and filtering. The +OUT connection should also be on plane layers to minimize inductance between DCM outputs. Control signal route lengths should be minimized but they should not be routed underneath the DCM body. This is especially true for EAO.

PMBus Interface

Refer to "PMBus Power System Management Protocol Specification Revision 1.3, Part I and II" for complete PMBus® specifications details visit http://pmbus.org

The DCM is a PMBus child and will respond only to host commands listed in this sections. Dedicated address (ADDR), Clock (SCL) and data (SDA) terminals are available; the optional SMBALERT# signal is not supported.

Device Address

The DCM PMBus address can be set using a 1% resistor from the ADDR terminal to ground. The following table lists the available addresses and the corresponding resistor value to use.

The DCM does not support SMBus Address Resolution protocol. The address is set at initial power up and then remains fixed until power is removed.

Restricted Address

The DCM also responds to address 0x50, but this address is for factory use only and cannot be used for any Supported Command in the list below. This address is fixed and cannot be changed. Care must be taken that no other device on the bus uses address 0x50 in order to avoid address collisions.

7-bit Hex Address	Resistor Value, 1% (kΩ)
20h	0.0
21h	12.1
22h	20.0
23h	28.0
24h	35.7
25h	44.2
26h	52.3
27h	open

Supported Command List and Supported Commands Transaction Type

Command Name	Command Code	Function	Default Data Content	SMBus Write Transaction	SMBus Read Transaction	Number of Data Bytes	Data Format	PEC
OPERATION	01h	Enable/disable control of DCM	84h	Write Byte	Read Byte	1	bit	Supported
CLEAR_FAULTS	03h	Clear fault status register	n/a	Write Byte	n/a	0	bit	Unsupported
STORE_USER_CODE	17h	Writes variable parameter to non-volatile memory	n/a	Write Byte	n/a	1	bit	Unsupported
CAPABILITY	19h	DCM key capabilities set by factory	A0h	n/a	Read Byte	1	bit	Supported
VOUT_MODE	20h	Format for VOUT_COMMAND	17h	n/a	Read Byte	1	bit	Supported
VOUT_COMMAND	21h	Set DCM output voltage	1C00h	Write Word	Read Word	2	ULINEAR16	Supported
VOUT_TRANSITION_RATE	27h	Set DCM output voltage slew rate in operation	F064h	Write Word	Read Word	2	LINEAR11	Supported
IOUT_OC_FAULT_LIMIT	46h	Set DCM constant current limit	F238h	Write Word	Read Word	2	LINEAR11	Supported
STATUS_BYTE	78h	Fault Readback	n/a	n/a	Read Byte	1	bit	Supported
STATUS_WORD	79h	Generic Fault Readback	n/a	n/a	Read Word	2	bit	Supported
READ_VIN	88h	DCM Input Voltage	n/a	n/a	Read Word	2	LINEAR11	Supported
READ_VOUT	8Bh	DCM Output Voltage	n/a	n/a	Read Word	2	ULINEAR16	Supported
READ_IOUT	8Ch	DCM Output Current	n/a	n/a	Read Word	2	LINEAR11	Supported
READ_TEMPERATURE_1	8Dh	DCM Temperature at Regulator Controller	n/a	n/a	Read Word	2	LINEAR11	Supported
MFR_ID	99h	Manufacturer ID	"VI"	n/a	Block Read	2	ASCII	Unsupported
IC_DEVICE_ID	ADh	Device Identification	"5160018"	n/a	Block Read	7	ASCII	Unsupported
MFR_STATUS_FAULTS	F0h	DCM Specific Faults	n/a	n/a	READ 32	4	bit	Supported

PMBus Command Definitions

A summary of the PMBus commands supported by the DCM are described in the following sections.

OPERATION Command (01h)

The OPERATION command and the DCM EN terminal can both be used to turn on and off the DCM. Default value is 84h at ON stage, and can be set to 04h for OFF stage.

Note that the Host OPERATION command will not enable the DCM if the DCM EN terminal is disabled in hardware with respect to the preset terminal polarity. The OPERATION command provides ON/OFF control only with the DCM EN terminal active.

If synchronous start up is required in the system, it is recommended to use the command from Host PMBus or the DCM EN terminal in order to achieve simultaneous array start up.

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re-asserted again once cleared, except for "$\overline{\text{FLT}}$ falling edge" bit, which is edge-triggered. All faults are latched once asserted in the DCM. Registered faults will not be cleared when the DCM powertrain is disabled through the $\overline{\text{FLT}}$ or EN terminal.

STORE_USER_CODE Command (17h)

STORE_USER_CODE can save the following command values to non-volatile memory. At subsequent power-ups, this stored value is used for the DCM.

For example, to store data of VOUT_COMMAND to non-volatile memory, the following transaction is sent: WRITE 0x17 0x21

STORE_USER_CODE can only be used NSTORE_USER_CODE times before all non-volatile memory is consumed.

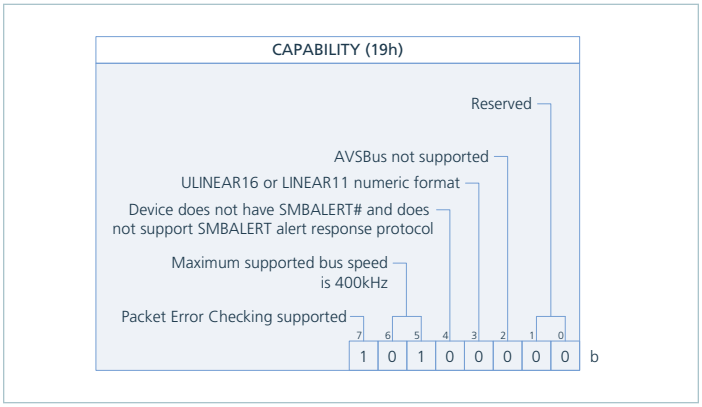
$N_{STORE\_USER\_CODE}$ = 8 (maximum)

Name	Code
OPERATION	0x01
VOUT_COMMAND	0x21
VOUT_TRANSITION_RATE	0x27
IOUT_OC_FAULT_LIMIT	0x46

CAPABILITY Command (19h)

The DCM returns a default value of A0h. This value indicates that the Packet Error Checking (PEC) is supported, PMBus® frequency is up to 400kHz, the SMBALERT# bit is not supported and that the numeric data can be LINEAR11 or ULINEAR16. See supported data command table indicating each command respective data reporting format.

Refer to the PMBus Power System Management Protocol Specification – Part II – Revision 1.3 for details on reported LINEAR11 and ULINEAR16 numeric format.



VOUT_MODE Command (20h)

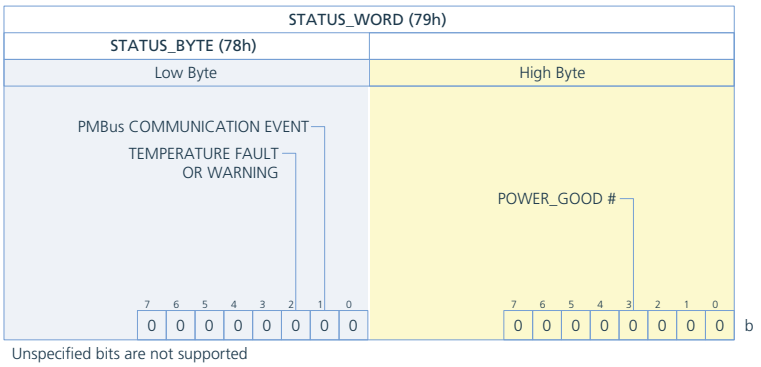
The DCM VOUT_MODE command is read-only. Set to a default value of 17h.

VOUT_COMMAND Command (21h)

VOUT_COMMAND causes the DCM to set the output voltage to the commanded value. Format is ULINEAR16 with –9 exponent, high byte, low byte. When multiple DCMs are used in parallel to create a high-power array, the group command protocol should be used when the VOUT_COMMAND is issued to change the output voltage. The group command protocol will cause all DCMs in the array to wait until the last unit receives the VOUT_COMMAND before collectively updating their output voltage setting. Not using the group command protocol can lead to nuisance detection of EAIN_HI faults for units which are programmed lower than the others in the array.

IOUT_OC_FAULT_LIMIT Command (46h)

The values of these registers are set in both volatile and non-volatile memory. The values of the above-mentioned constant-current mode level are set by default to 142A (F238h) of the respective DCM model limits at 14V. However, these limits can be set to other values. For example: In order for a limit to be set to 80A, one would send a write command with a (F140h) Data Word.



Unspecified bits are not supported

STATUS_BYTE (78h) and STATUS_WORD (79h)

Although the DCM powertrain will self-restart once fault conditions are cleared, all fault or warning flags, if set, will remain asserted until cleared by the host or once DCM input power is removed. This includes overtemperature warning and communication faults.

STATUS_WORD and STATUS_BYTE can be cleared by sending CLEAR_FAULTS (03h) command.

The TEMPERATURE FAULT bit reflects that an overtemperature shut down of the Stage 1 ZVS buck-boost occurred.

The PMBus® COMMUNICATION EVENT bit is set when a communication fault occurs. See the PMBus Communication Fault section for details.

READ_VIN Command (88h)

READ_VIN returns the input voltage telemetry in LINEAR11 format.

READ_VOUT Command (8Bh)

READ_VOUT returns the output voltage telemetry in ULINEAR16 format. Refer to the PMBus Power System Management Protocol Specification – Part II – Revision 1.3 for details on reported LINEAR11 and ULINEAR16 numeric format.

READ_IOUT Command (8Ch)

READ_IOUT returns the output current telemetry in LINEAR11 format.

READ_TEMPERATURE_1 (8Dh)

READ_TEMPERATURE_1 returns the measured temperature at the stage 1 ZVS buck-boost controller. This temperature can be used as a relative gauge to the operating temperature of one internal area of the module.

READ_TEMPERATURE_1 is not sufficient to design or validate any module-level thermal solution. Thermal design must use the module power dissipation and thermal resistance model to ensure that all areas of the module internal circuitry are kept below the maximum operating temperature.

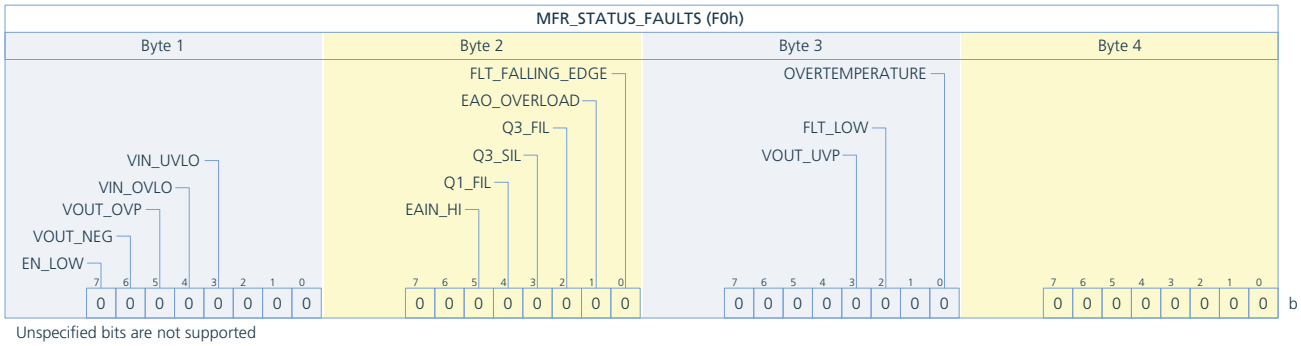
MFR_ID (99h)

This read-only command will return “VI” as two ASCII bytes, indicating the manufacturer Vicor Corporation.

MFR_STATUS_FAULTS (F0h)

This command returns four bytes; the first three are used and are defined in the table above. All fault or warning flags, if set, will remain asserted until cleared by the host. A CLEAR_FAULTS (03h) command should be issued after power is initially applied to clear any fault flags which are set during module initialization.

Note: For information detailing detection and response to specific faults, see Functional Description section.



Unspecified bits are not supported

PMBus Communication Fault

Module Behavior

Corrupted data, unrecognized commands, or other PMBus® protocol violations have no impact on powertrain functionality.

PMBus Reporting Characteristics

The below tables summarize data transmission faults and data content faults as implemented in the DCM.

Data Transmission Faults Implementation

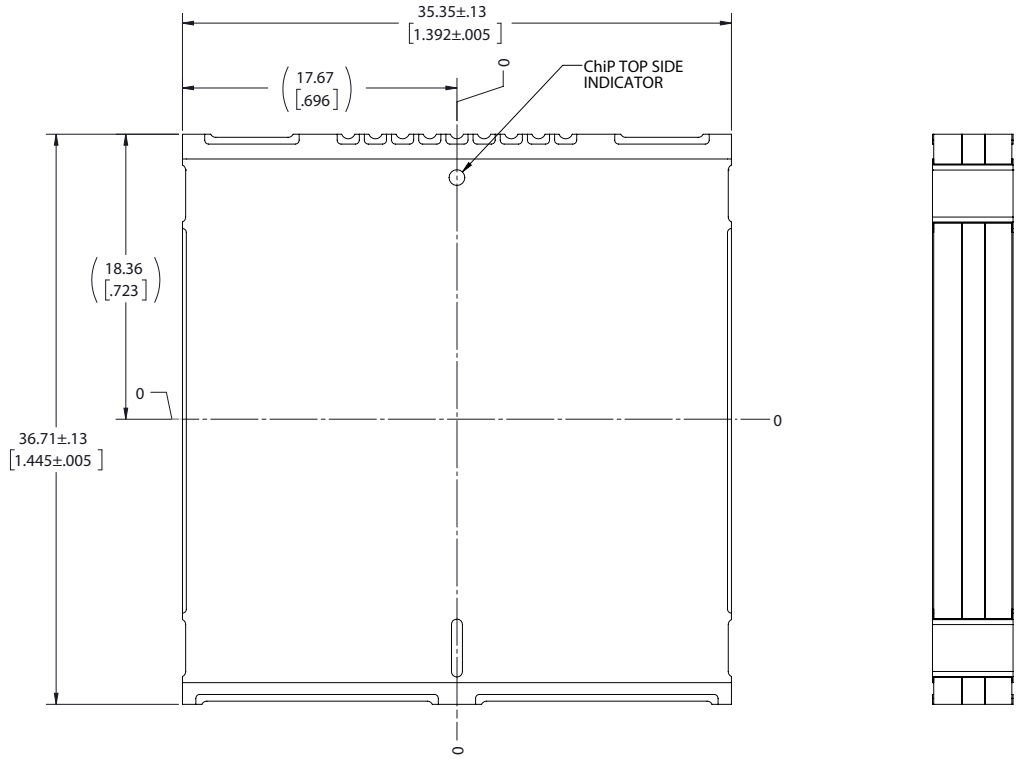
Section	Description	STATUS_BYTE	Notes
		CML	
10.8.1	Corrupted data	X	PEC failure
10.8.2	Sending too few bits		Device will ignore transmission
10.8.3	Reading too few bits		No response
10.8.4	Host sends or reads too few bytes	X	CML set on writes only
10.8.5	Host sends too many bytes	X	
10.8.6	Reading too many bytes		Read will report old data
10.8.7	Device busy		Clock stretch prior to ACK

Data Content Faults Implementation

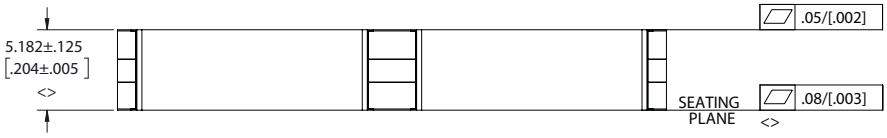
Section	Description	STATUS_BYTE	Notes
		CML	
10.9.1	Improperly set read bit in the address byte		Not interpreted as a fault; device will respond normally
10.9.2	Unsupported command code	X	
10.9.3	Invalid or unsupported data	X	
10.9.4	Data out of range		No response
10.9.5	Reserved bits		No response; not a fault

Product Outline Drawing – Top View

DCM3735 TC2
(Reference DWG # 49838 Rev 4)



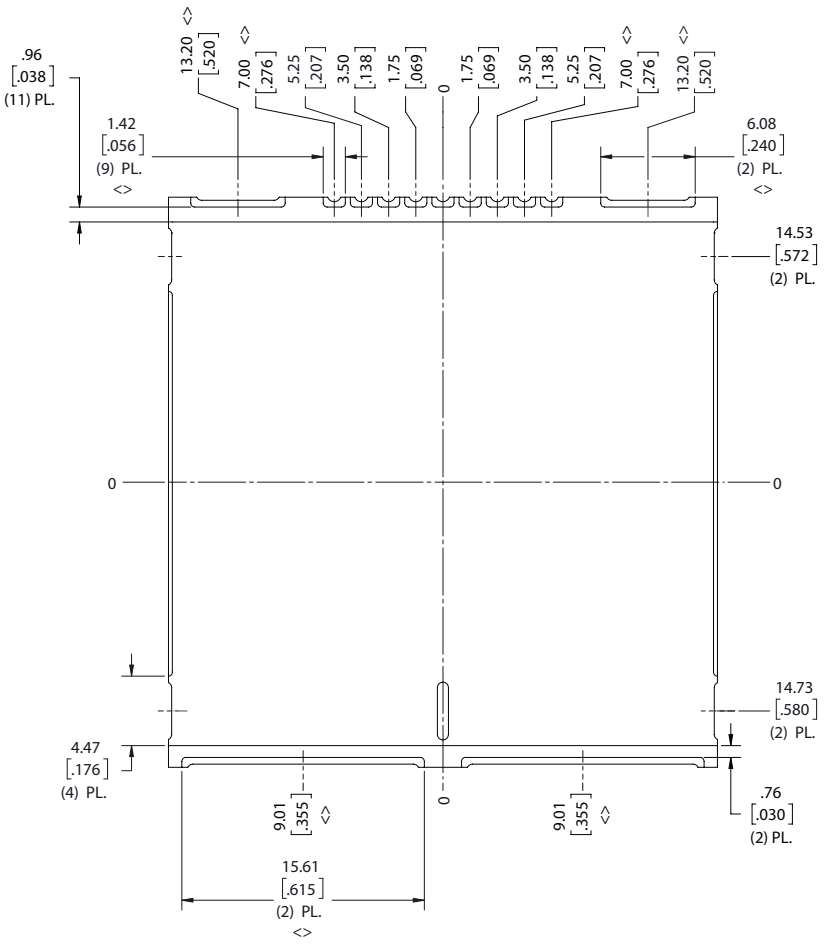
TOP VIEW
(COMPONENT SIDE)



NOTES:
1- <> DENOTES CRITICAL CHARACTERISTIC
2- UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM [INCH]
3- TOLERANCES ARE:
DECIMALS
X.XX [X.XX] = ±0.25 [0.01]
X.XXX [X.XXX] = ±0.127 [0.005]
ANGLES = ±1°

Product Outline Drawing – Bottom View

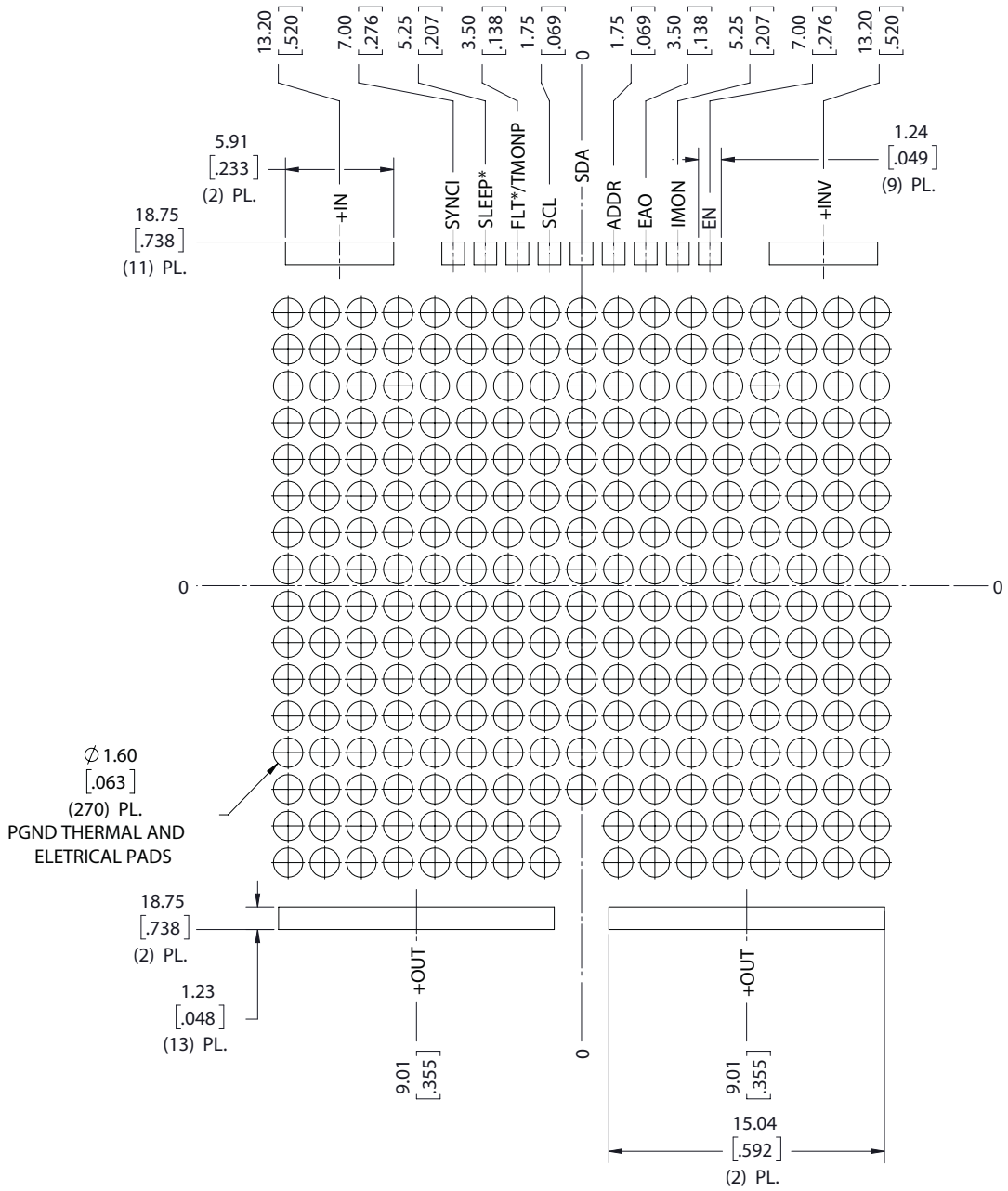
DCM3735 TC2
(Reference DWG # 49838 Rev 4)



BOTTOM VIEW

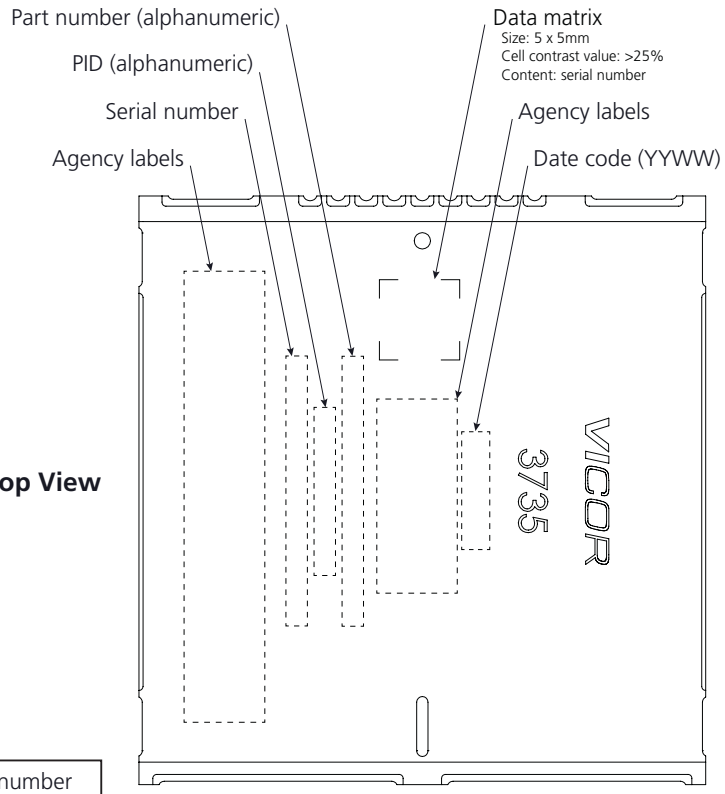
Recommended Land Pattern

DCM3735 TC2
(Reference DWG # 49838 Rev 4)



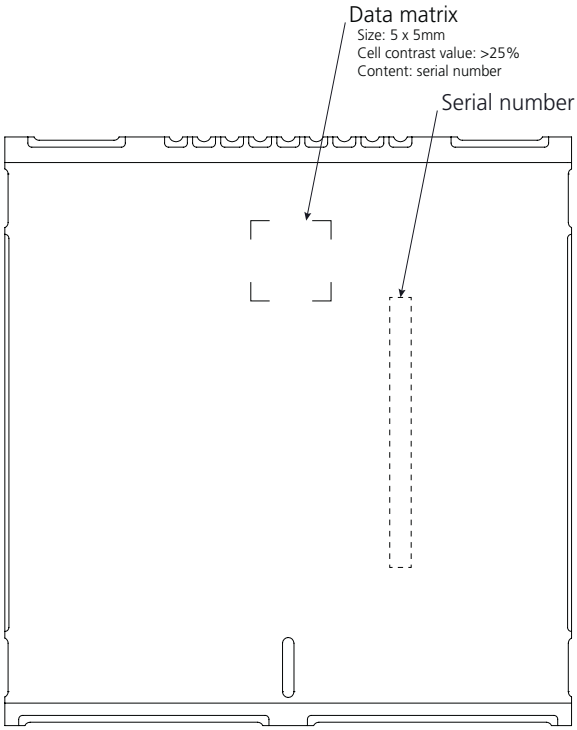
RECOMMENDED LAND PATTERN
(COMPONENT SIDE)

Package Marking Specification



Top View

Example 16-digit serial number
A 023 10 04 00004143
Year (2023)
Month (October)
Day (4th)
Module count (4143rd of this day)



Bottom View

Revision History

Revision	Date	Description	Page Number(s)
1.0	04/25/24	Initial release	n/a
1.1	06/11/24	Updated typical application diagrams Updated absolute max rating for $\overline{\text{SLEEP}}$ Updated I_{OC} minimum Updated thermal operating area, added thermal design power dissipation Added no-load performance Corrected SMBus write transation for OPERATION, CLEAR_FAULTS Updated diagram format: STATUS_BYTE, STATUS_WORD, MFR_STATUS_FAULTS	2 4 7 11, 24 15 26 28
1.2	07/30/24	Updated outline drawing	30, 31, 32
1.3	10/07/24	Updated features and benefits	1

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