Dual-Stage Feedback Technique for Single-Pole Feedback Compensation

Joseph Aguilar

Abstract

This paper proposes and studies the effects of a dual-stage compensation technique for achieving greater than 100kHz crossover frequency of a single-pole system converting from 48 to 1.2V. By placing a separate non-inverting gain stage after the error amplifier, the necessary gain-bandwidth of the op amp can be significantly reduced allowing for high crossover frequency and good transient response.

Background

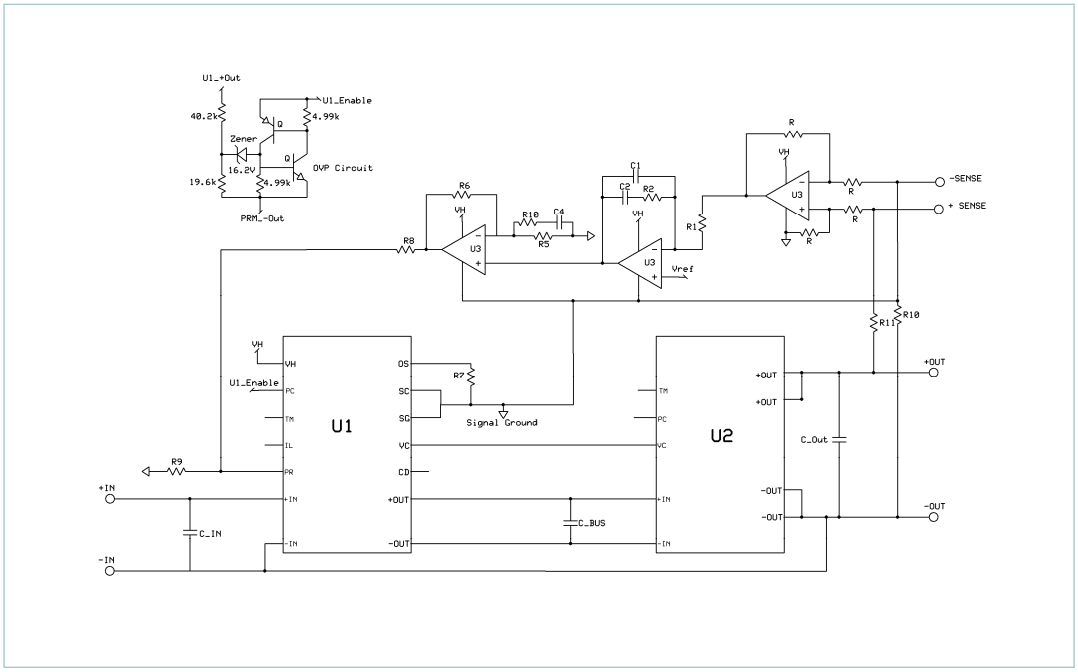
Previous work has proposed a power conversion architecture for 48V inputs to sub-volt loads consisting of a Sine Amplitude Converter (SAC™) providing voltage transformation / current multiplication at the load, with an upstream Zero-Voltage Switched (ZVS) buck-boost regulator providing remote regulation at the point-of-load. [a] The low impedance characteristic of the sine amplitude converter was evaluated in detail and the capability of the ZVS buck-boost stage to provide high-bandwidth regulation was established. The actual design of a high-bandwidth feedback loop was left as a topic of future work. This paper analyzes the effect of a dual-stage feedback loop in the implementation of a high-bandwidth control loop feeding back to a ZVS buck-boost regulator.

The standard approach for designing a high-bandwidth closed-loop system using a single amplifier with a high gain-bandwidth product. [b]

For a target bandwidth of 100kHz, a gain-bandwidth of 80 – 100MHz would be appropriate.

The proposed approach uses two lower-bandwidth amplifiers to provide 100kHz closed-loop bandwidth with DC and mid-band gain of 40dB or greater. The first amplifier stage provides the error amplifier function with Type 2 compensation (pole at the origin, zero for mid-band gain, pole at high frequency). The second amplifier provides DC gain with the option of a second zero at high frequency.

Figure 1
48 – 1.2V, 100A



Power conversion

This approach uses two power components and a voltage feedback loop as shown in Figure 1. The output voltage and current capability of this implementation is 1.2V and 100A.

U1 is the ZVS buck-boost regulator. [c] The output power is controlled by its control pin (PR). The voltage at this pin will result in a DC output determined by the modulator gain, which is a function of line and load. The switching frequency of this device is nominally 1.0MHz. [c] The output of U1 is connected to a sine amplitude converter (U2) which provides fixed-ratio conversion determined by its internal turns ratio. [d] For a 1.2V output voltage, a turns ratio of 1/32 (–30dB) is used. The switching frequency of U2 is nominally 1.4MHz. [d] Although U2 contains an isolated output, this implementation does not contain input to output isolation. This is done in order to maximize the feedback-loop bandwidth by circumventing the need for feedback-isolating devices.

Power component frequency response

The ZVS buck-boost regulator (U1) frequency response consists of a single pole determined by the output capacitance and equivalent load resistance as described by Equation 1. [e] The DC gain is typically between 20 and 30dB and varies with line and load.

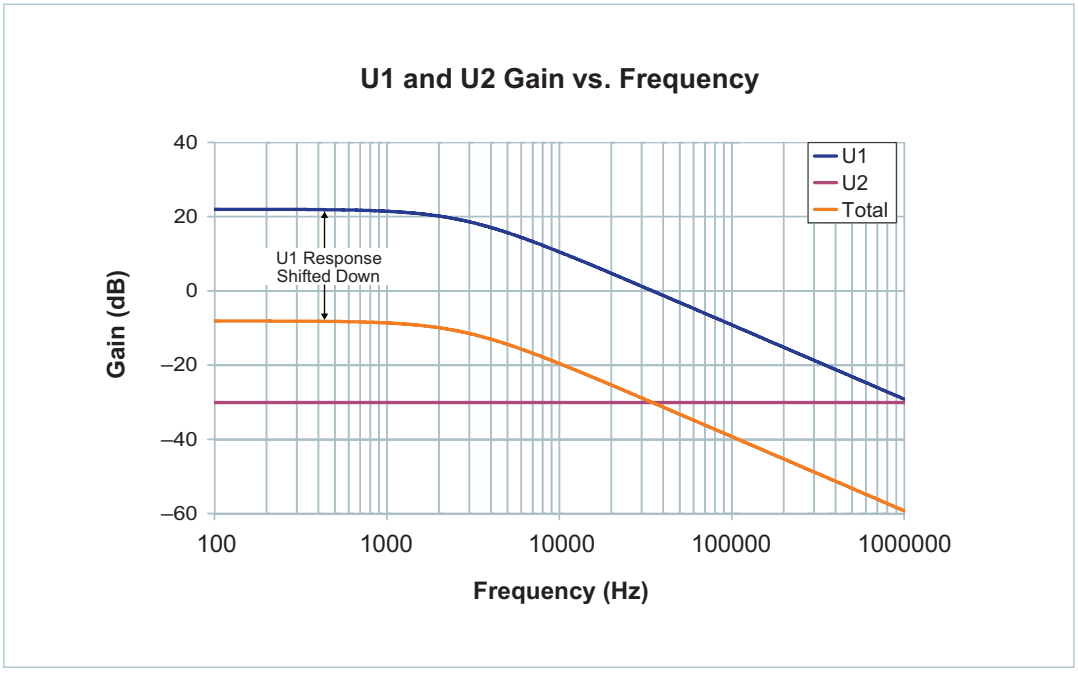
$$F_{POLE\_U1} = \frac{1}{2\pi \bullet R_{OUT\_U1} \bullet C_{OUT\_U1}} = \frac{1}{2\pi \bullet \frac{V_{OUT\_U1}}{I_{OUT\_U1}} \bullet C_{OUT\_U1}} \quad (1)$$

The sine amplitude converter (U2) gain is assumed fixed vs. frequency with a value determined by the turns ratio.

$$G_{U2} = 20log_k = 20log\left(\frac{V_{OUT\_U2}}{V_{IN\_U2}}\right) \quad (2)$$

The resulting gain vs. frequency response for each device is illustrated in Figure 2. The overall response is determined by adding the two together. Second-order effects are not included in this analysis. During validation of this approach, it was discovered that these effects influence the closed-loop response starting at 60kHz and need to be analyzed in greater detail. Further discussion of the second-order effects are included in the conclusion.

Figure 2
U1 and U2 frequency response

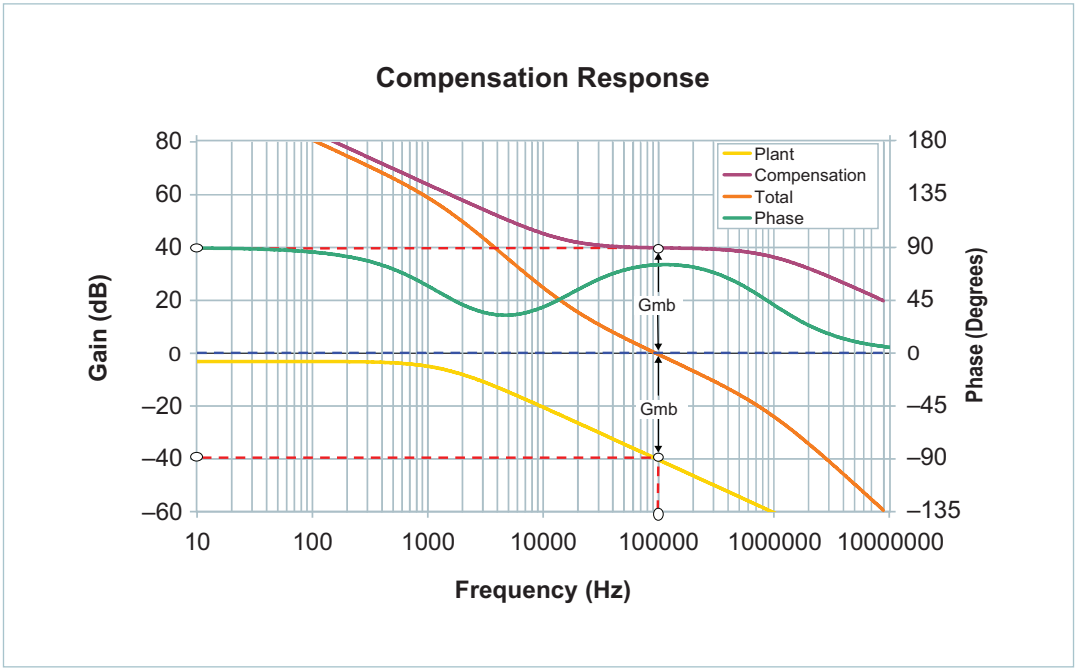


Compensation technique

High-frequency (>100kHz) crossover

The high switching frequency of U1 and U2 enable a closed-loop crossover frequency of between 100 – 300kHz maximum. [f] By examining the powertrain plant, the characteristic response of the compensation can be determined for a high crossover frequency with adequate phase margin. At 100kHz, the gain of the plant response is typically between –35 and –40dB. For a 100kHz crossover frequency, the gain of the compensation stage must therefore be between 35 and 40dB at this frequency. A zero prior to the crossover frequency is necessary to bring the phase margin above 45 degrees and change the slope of the gain to –20dB/decade. An additional high-frequency pole is introduced prior to the gain-bandwidth limit of the feedback amplifier. This pole should be placed at least one decade above the desired crossover to avoid degradation to the phase margin. The proposed compensation response is illustrated in Figure 3.

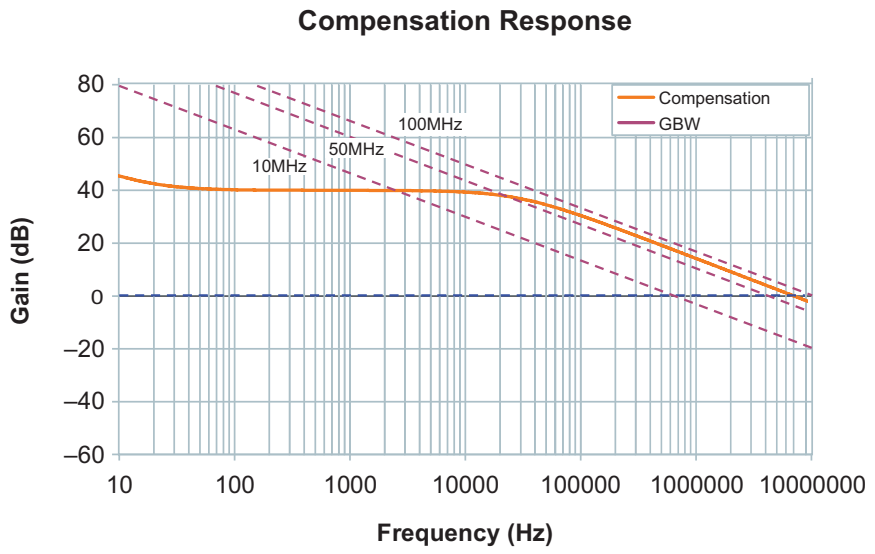
Figure 3
Proposed compensation response



Feedback Amplifier Gain-Bandwidth

The effect of the feedback amplifier gain-bandwidth product is illustrated in Figure 4. As the gain of the feedback amplifier is increased in order to provide higher crossover frequency, the necessary gain-bandwidth product of the feedback amplifier must be increased to avoid detrimental effects due to this pole. As illustrated, for the proposed crossover frequency of 100kHz, a gain-bandwidth product of between 80 and 100MHz would be necessary. Also critical to the response is the output slew rate of the amplifier, compared with the required slew range. Finding an amplifier with an appropriate gain-bandwidth product and slew rate can be challenging. In addition to this, many high gain-bandwidth amplifiers are not suited to being used as feedback error amplifiers and are difficult to stabilize at lower frequencies, especially within the feedback loop, i.e., less than 100kHz.

Figure 4
Feedback amplifier gain-bandwidth product



Dual-stage compensation circuit

The proposed compensation circuitry is illustrated in Figure 5. The first op amp is used as a differential sense amplifier with a gain of one. The second provides the error amplifier function with type-2 compensation for the necessary poles and zeros. A third amplifier is added with a fixed gain following the error amplifier. By adding this additional gain amplifier, the mid-band gain can be broken into two stages reducing the necessary gain-bandwidth product of the op amp. As an example, the amplifier gains are each set to 20dB for a total of 40dB at the desired crossover. The necessary amplifier gain-bandwidth product can now be reduced to 10MHz as illustrated in Figure 6.

Figure 5
Dual-stage compensation circuit

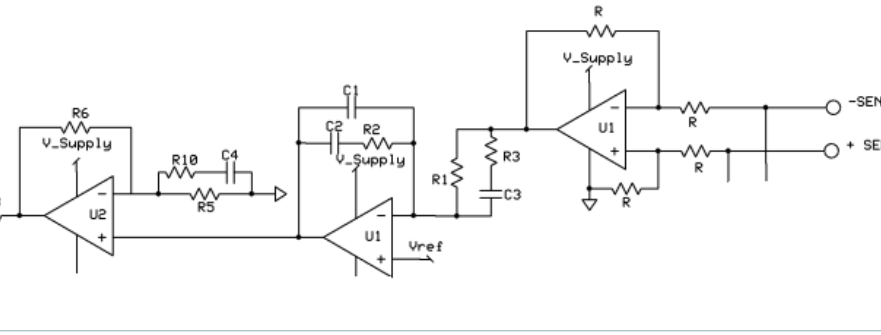
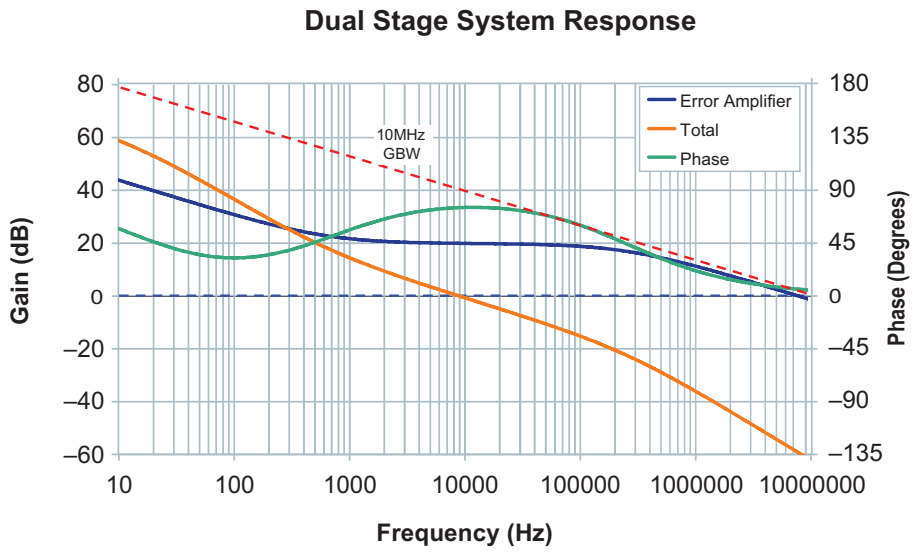


Figure 6
Dual-stage compensation response



In addition to reducing the gain-bandwidth of the op amp, it is proposed that the DC gain stage will have a positive effect on the load transient response. The ZVS buck-boost regulator control signal has an active range of 1 – 5V. The compensation components in the error amplifier limit the slew rate of the error amplifier depending on the component R-C time constants. The DC gain stage reduces the necessary slew range of the error amplifier during load transients improving the large signal response of the control loop.

Pole-zero placement

The proposed error amplifier compensation consists of two poles and one zero.

The first pole F_{PDC} begins at the origin with 0dB gain defined by Equation 3. The compensator zero is defined by Equation 4. The second pole is defined by Equation 5. The mid-band gain of the error amplifier is defined by Equation 6. This is the gain between F_{Z1} and F_{P1} where the response is constant vs. frequency. The gain of the non-inverting amplifier is defined by Equation 7. This gain is constant vs. frequency until it crosses the gain-bandwidth limit of the op amp.

$$F_{PDC} = \frac{1}{2\pi \bullet R1 \bullet (C1 + C2)} \quad (3)$$

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C1} \quad (4)$$

$$F_{P1} = \frac{1}{2\pi \bullet \frac{R2 \bullet C1 \bullet C2}{C1 + C2}} \quad (5)$$

$$G_{MB} = \frac{R2}{R1} \quad (6)$$

$$G_{DC} = 1 + \frac{R6}{R5} \quad (7)$$

The procedure for selecting the components is as follows:

1. Determine the load at which the plant response is at a maximum.
2. Determine the gain of the plant at the desired crossover frequency using the maximum plant response.
3. Determine the necessary compensation gain in order to shift the plant up to 0dB at the desired crossover frequency.
4. Set the mid-band gain of the error amplifier to half of this gain.
5. Set the DC gain equal to the error amplifier mid-band gain.
6. Determine the minimum crossover frequency of the system based on the minimum plant response. This is typically between 30 – 40kHz below the maximum.
7. Set the compensation zero F_{Z1} prior to the minimum crossover frequency.
8. Set the second compensation pole F_{P1} at least one decade above the maximum crossover frequency, and prior to the gain-bandwidth limit of the op amp.

Results

Frequency response

The above describe technique was implemented in a laboratory environment using actual components in order to achieve the highest allowable crossover frequency. The test set up is shown in Figure 7. A quad 10MHz gain-bandwidth op amp was used as the differential sense amplifier, error amplifier, and gain amplifier. 300µF of ceramic capacitance was placed at the output of the sine amplitude converter. The resulting gain and phase plot of the system is shown in Figure 8. The maximum crossover achieved was 72kHz with a phase margin of 43 degrees. The required gain of the compensation was approximately 30dB, with a compensator zero at 20kHz.

Figure 7
Experimental set up

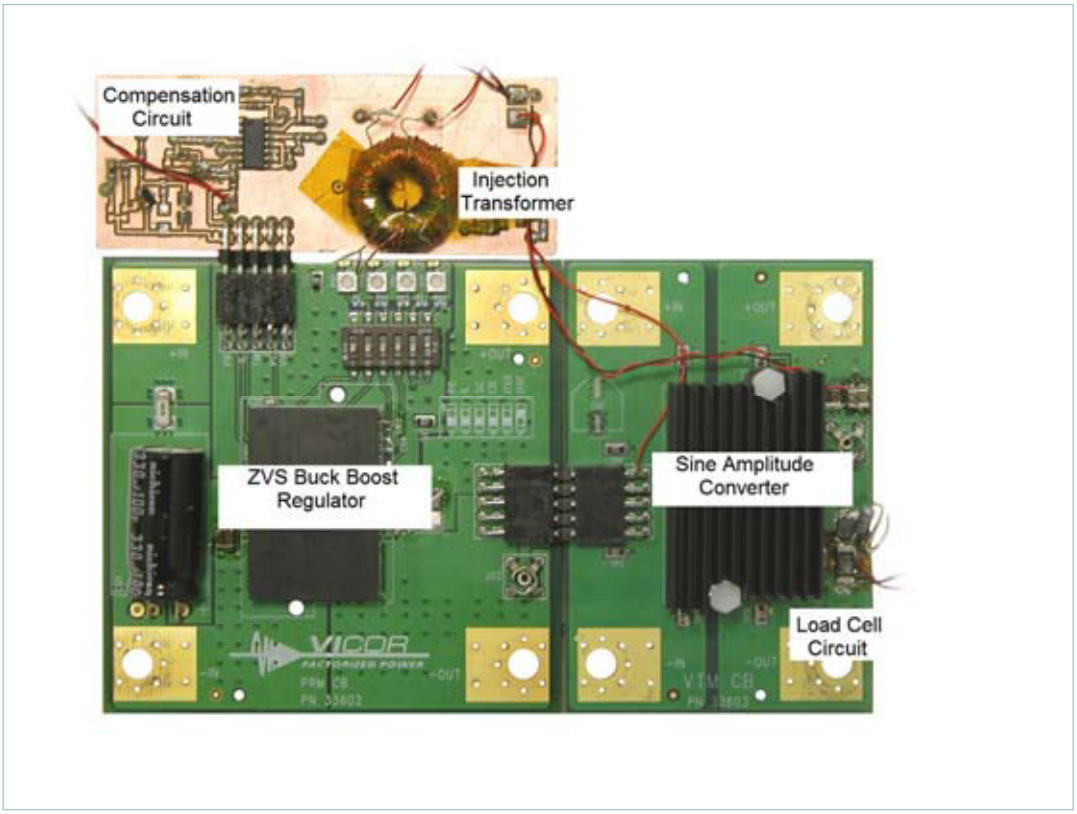
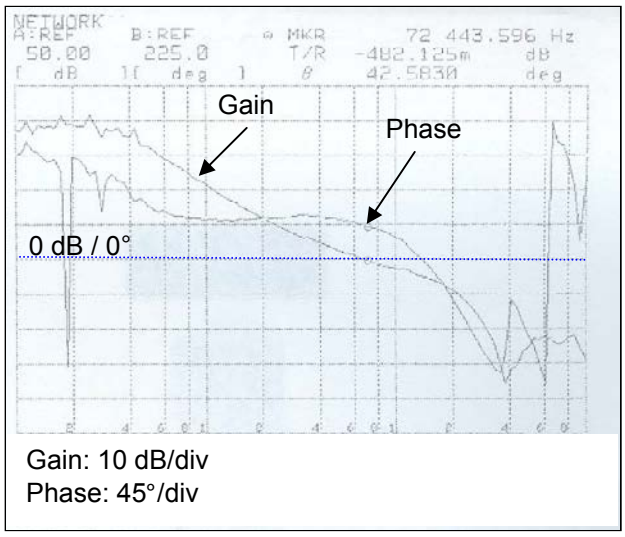


Figure 8
Experimental frequency response



Transient response

A FET load circuit illustrated in Figure 9 was used to generate a high-current, high-dI/dt-load step to measure the system transient response. The rise time of the current was controlled through a function generator. The current waveform is sensed across a 15mΩ current sense resistor and the output voltage measured directly at the output of the Sine Amplitude Converter (SAC™).

The resulting transient response waveform to a 50A, 50A/µs load step is shown in Figure 10. The total undershoot is 50mV with a recovery time of 5µs.

Figure 9
FET load-switch circuit

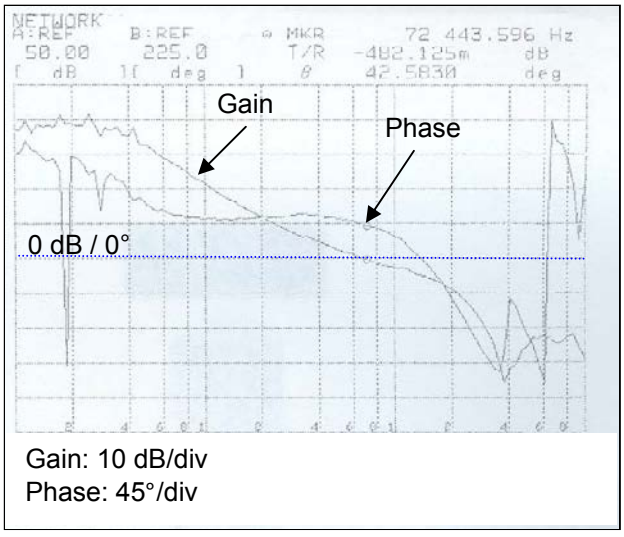
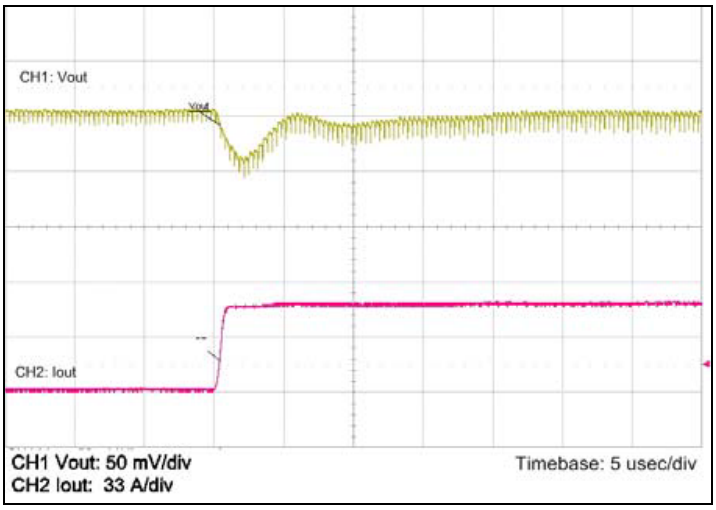


Figure 10
30 – 80A Transient Response of 48 – 1.2V converter. 300µF of ceramic output capacitance



Effect of dual-stage technique on transient response

The effect of the additional DC gain stage on transient response was evaluated. The gain stage was removed and the loop recompensated for the same crossover frequency and pole-zero locations. Although the expectation was that the transient response would be degraded, the results showed that the difference in performance was not significant. Overall the system is capable of exceptional transient response and recovery time regardless of whether or not the gain stage was added. It is theorized that the effect of the gain stage would have been more significant if the overall loop bandwidth was higher.

Conclusion

These results indicate identical system behavior whether or not a second gain amplifier stage is used in the compensation circuit.

This is likely due to the fact that the actual crossover frequency for this system was less than 100kHz. As illustrated in Figure 8, higher order effects limited the maximum system-crossover frequency in this particular implementation. The phase of the system is degraded starting at 60kHz, leading to poor phase margin above the measured crossover frequency. In addition, the slope of the system gain begins to decrease at around 80kHz, leading to poor gain margin and preventing the use of a second zero after the crossover to improve the phase.

The cause of these effects is not known, but is likely due to one or more of the following:

1. Series impedance between the U1 and U2 creating an LC filter in the plant response with a corner frequency around 500KHz, thus introducing phase degradation at 60kHz.
2. Uncharacterized parasitic impedances due to the layout of the system which include twisted wires, connector and inductance at the output of U2.

Future work will focus on investigating the cause of these higher-order effects. Improvements will be made to reduce the impedance of the Sine Amplitude Converter (SAC™) and a dedicated board will be designed containing all of the necessary components, reducing parasitic effects.

Literature

[a] Yeaman, Paul, "High Current, Low Voltage Solution For Microprocessor Applications from 48V Input"*, PCIM 2007*.

[b] Analog Devices, *Low Cost, High Speed Rail-to-Rail Amplifiers AD8091/AD8092*, http://www.analog.com/media/en/technical-documentation/data-sheets/AD8091_8092.pdf

[c] VI Chip *PRM P045F048T32AL* data sheet, http://www.vicorpower.com/products?productType=cfg&productKey=P045F048T32AL

[d] VI Chip *VTM V048F015T100* data sheet, http://www.vicorpower.com/products?productType=cfg&productKey=V048F015T100

[e] Vinciarelli, P., "Buck-boost DC--DC switching power conversion", U.S. Patent 7,154,250. Issued December 26, 2006" to this citation. https://patents.justia.com/patent/7154250

[f] Pressman, A., *Switching Power Supply Design*, ISBN 0-07-050806-2

Contact Us: http://www.vicorpower.com/contact-us

Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715
www.vicorpower.com

email
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com